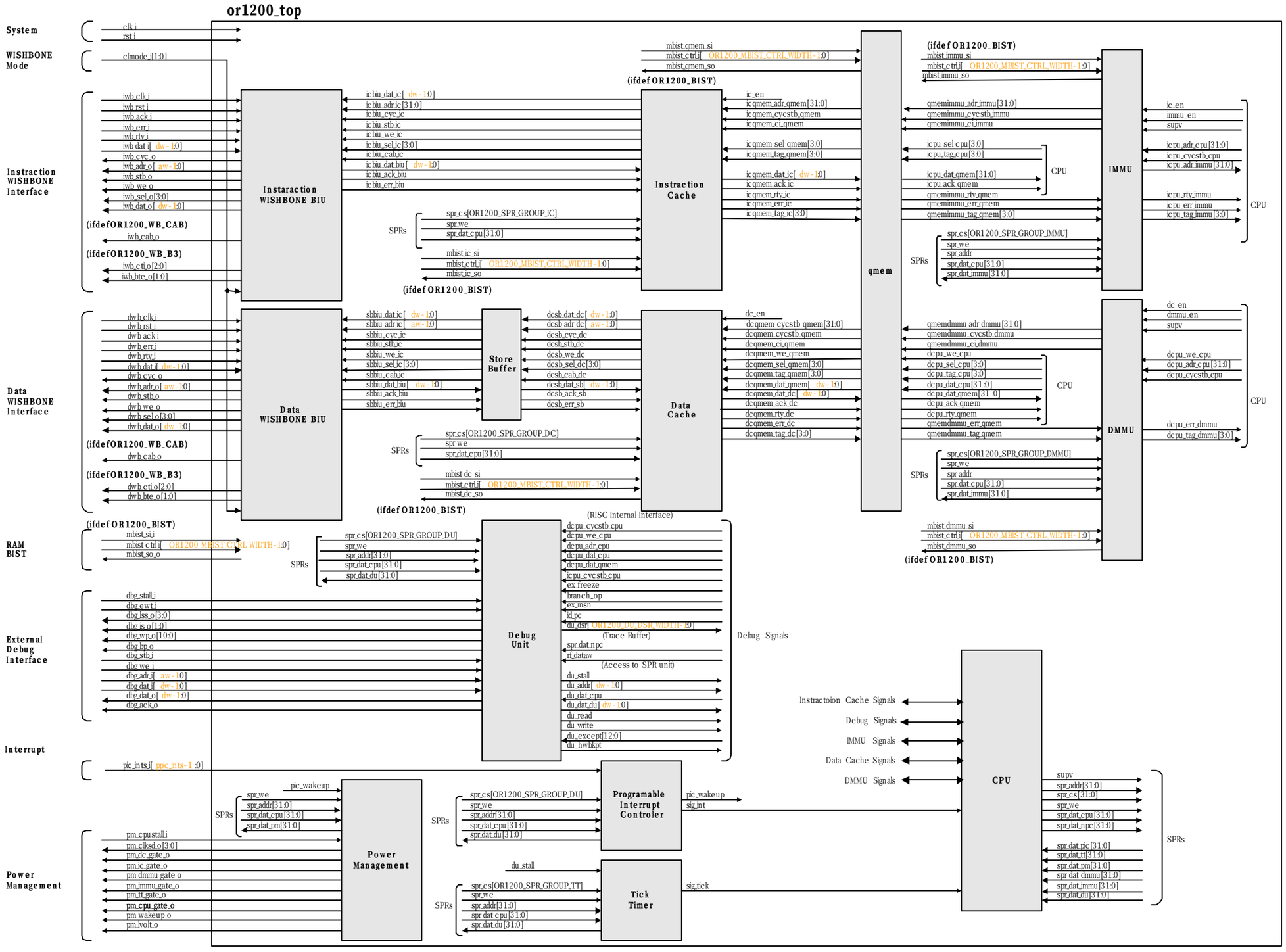
or1200 core


or1200_top
System
clk_i
rst_i
WISHBONE Mode
clmode_i[1:0]
Instraction WISHBONE Interface
iwb_clk_i
iwb_rst_i
iwb_ack_i
iwb_err_i
iwb_rty_i
iwb_dat_i[dw - 1:0]
iwb_cyc_o
iwb_adr_o[aw - 1:0]
iwb_stb_o
iwb_we_o
iwb_sel_o[3:0]
iwb_dat_o[dw - 1:0]
(ifdef OR1200_WB_CAB)
iwb_cab_o
(ifdef OR1200_WB_B3)
iwb_cti_o[2:0]
iwb_bte_o[1:0]
Data WISHBONE Interface
dwb_clk_i
dwb_rst_i
dwb_ack_i
dwb_err_i
dwb_rty_i
dwb_dat_i[dw - 1:0]
dwb_cyc_o
dwb_adr_o[aw - 1:0]
dwb_stb_o
dwb_we_o
dwb_sel_o[3:0]
dwb_dat_o[dw - 1:0]
(ifdef OR1200_WB_CAB)
dwb_cab_o
(ifdef OR1200_WB_B3)
dwb_cti_o[2:0]
dwb_bte_o[1:0]
(ifdef OR1200_BIST)
RAM BIST
mbist_si_i
mbist_ctrl_i[OR1200_MBIST_CTRL_WIDTH - 1:0]
mbist_so_o
External Debug Interface
dbg_stall_i
dbg_ewt_i
dbg_lss_o[3:0]
dbg_is_o[1:0]
dbg_wp_o[10:0]
dbg_bp_o
dbg_stb_i
dbg_we_i
dbg_adr_i[aw - 1:0]
dbg_dat_i[dw - 1:0]
dbg_dat_o[dw - 1:0]
dbg_ack_o
Interrupt
pic_ints_i[ppic_ints - 1 :0]
Power Management
pm_cpu stall_i
pm_clksd_o[3:0]
pm_dc_gate_o
pm_ic_gate_o
pm_dmmu_gate_o
pm_immu_gate_o
pm_tt_gate_o
pm_cpu_gate_o
pm_wakeup_o
pm_lvolt_o
Instaraction WISHBONE BIU
ic biu_dat_ic[dw - 1:0]
ic biu_adr_ic[31:0]
ic biu_cyc_ic
ic biu_stb_ic
ic biu_we_ic
ic biu_sel_ic[3:0]
ic biu_cab_ic
ic biu_dat_biu[dw - 1:0]
ic biu_ack_biu
ic biu_err_biu
Data WISHBONE BIU
sbbiu_dat_ic[dw - 1:0]
sbbiu_adr_ic[aw - 1:0]
sbbiu_cyc_ic
sbbiu_stb_ic
sbbiu_we_ic
sbbiu_sel_ic[3:0]
sbbiu_cab_ic
sbbiu_dat_biu[dw - 1:0]
sbbiu_ack_biu
sbbiu_err_biu
Store Buffer
dcsb_dat_dc[dw - 1:0]
dcsb_adr_dc[aw - 1:0]
dcsb_cyc_dc
dcsb_stb_dc
dcsb_we_dc
dcsb_sel_dc[3:0]
dcsb_cab_dc
dcsb_dat_sb[dw - 1:0]
dcsb_ack_sb
dcsb_err_sb
SPRs
spr_cs[OR1200_SPR_GROUP_IC]
spr_we
spr_dat_cpu[31:0]
mbist_ic_si
mbist_ctrl_i[OR1200_MBIST_CTRL_WIDTH - 1:0]
mbist_ic_so
(ifdef OR1200_BIST)
spr_cs[OR1200_SPR_GROUP_DC]
spr_we
spr_dat_cpu[31:0]
mbist_dc_si
mbist_ctrl_i[OR1200_MBIST_CTRL_WIDTH - 1:0]
mbist_dc_so
(ifdef OR1200_BIST)
Instraction Cache
ic_en
icqmem_adr_qmem[31:0]
icqmem_cycstb_qmem
icqmem_ci_qmem
icqmem_sel_qmem[3:0]
icqmem_tag_qmem[3:0]
icqmem_dat_ic[dw - 1:0]
icqmem_ack_ic
icqmem_rty_ic
icqmem_err_ic
icqmem_tag_ic[3:0]
Data Cache
dc_en
dcqmem_cycstb_qmem[31:0]
dcqmem_cycstb_qmem
dcqmem_ci_qmem
dcqmem_we_qmem
dcqmem_sel_qmem[3:0]
dcqmem_tag_qmem[3:0]
dcqmem_dat_qmem[dw - 1:0]
dcqmem_dat_dc[dw - 1:0]
dcqmem_ack_dc
dcqmem_rty_dc
dcqmem_err_dc
dcqmem_tag_dc[3:0]
Debug Unit
(RISC Internal Interface)
dcpu_cycstb_cpu
dcpu_we_cpu
dcpu_adr_cpu
dcpu_dat_cpu
dcpu_dat_qmem
icpu_cycstb_cpu
ex_freeze
branch_op
ex_insn
id_pc
du_dsr[OR1200_DU_DSR_WIDTH - 1:0]
(Trace Buffer)
spr_dat_npc
rf_dataw
(Access to SPR unit)
du_stall
du_addr[dw - 1:0]
du_dat_cpu
du_dat_du[dw - 1:0]
du_read
du_write
du_except[12:0]
du_hwbkpt
Debug Signals
qmem
(ifdef OR1200_BIST)
mbist_qmem_si
mbist_ctrl_i[OR1200_MBIST_CTRL_WIDTH - 1:0]
mbist_qmem_so
(ifdef OR1200_BIST)
mbist_immu_si
mbist_ctrl_i[OR1200_MBIST_CTRL_WIDTH - 1:0]
mbist_immu_so
qmemimmu_adr_immu[31:0]
qmemimmu_cycstb_immu
qmemimmu_ci_immu
icpu_sel_cpu[3:0]
icpu_tag_cpu[3:0]
icpu_dat_qmem[31:0]
icpu_ack_qmem
qmemimmu_rty_qmem
qmemimmu_err_qmem
qmemimmu_tag_qmem[3:0]
SPRs
spr_cs[OR1200_SPR_GROUP_IMMU]
spr_we
spr_addr
spr_dat_cpu[31:0]
spr_dat_immu[31:0]
IMMU
ic_en
immu_en
supv
icpu_adr_cpu[31:0]
icpu_cycstb_cpu
icpu_adr_immu[31:0]
icpu_rty_immu
icpu_err_immu
icpu_tag_immu[3:0]
CPU
qmemdmmu_adr_dmmu[31:0]
qmemdmmu_cycstb_dmmu
qmemdmmu_ci_dmmu
dcpu_we_cpu
dcpu_sel_cpu[3:0]
dcpu_tag_cpu[3:0]
dcpu_dat_cpu[31:0]
dcpu_dat_qmem[31:0]
dcpu_ack_qmem
dcpu_rty_qmem
qmemdmmu_err_qmem
qmemdmmu_tag_qmem
SPRs
spr_cs[OR1200_SPR_GROUP_DMMU]
spr_we
spr_addr
spr_dat_cpu[31:0]
spr_dat_immu[31:0]
DMMU
dc_en
dmmu_en
supv
dcpu_we_cpu
dcpu_adr_cpu[31:0]
dcpu_cycstb_cpu
dcpu_err_dmmu
dcpu_tag_dmmu[3:0]
CPU
mbist_dmmu_si
mbist_ctrl_i[OR1200_MBIST_CTRL_WIDTH - 1:0]
mbist_dmmu_so
(ifdef OR1200_BIST)
Instractoion Cache Signals
Debug Signals
IMMU Signals
Data Cache Signals
DMMU Signals
CPU
supv
spr_addr[31:0]
spr_cs[31:0]
spr_we
spr_dat_cpu[31:0]
spr_dat_npc[31:0]
spr_dat_pic[31:0]
spr_dat_tt[31:0]
spr_dat_pm[31:0]
spr_dat_dmmu[31:0]
spr_dat_immu[31:0]
spr_dat_du[31:0]
SPRs
Power Management
pic_wakeup
SPRs
spr_we
spr_addr[31:0]
spr_dat_cpu[31:0]
spr_dat_pm[31:0]
Programable Interrupt Controler
spr_cs[OR1200_SPR_GROUP_DU]
spr_we
spr_addr[31:0]
spr_dat_cpu[31:0]
spr_dat_du[31:0]
pic_wakeup
sig_int
Tick Timer
du_stall
spr_cs[OR1200_SPR_GROUP_TT]
spr_we
spr_addr[31:0]
spr_dat_cpu[31:0]
spr_dat_du[31:0]
sig_tick