

FL-850/FG4
FL-850/FG4-S
Hardware Manual

Date published: January 2012 (First Edition)

Tessera Technology Inc.

CAUTION:

- The information in this document is subject to change without notice.
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of Tessera Technology Inc.
- Tessera Technology Inc. assumes no responsibility for inaccuracies or misprints of this document.
- Tessera Technology Inc. does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of Tessera Technology Inc. products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of Tessera Technology Inc. or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of a customer's equipment shall be done under the full responsibility of the customer. Tessera Technology Inc. assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.

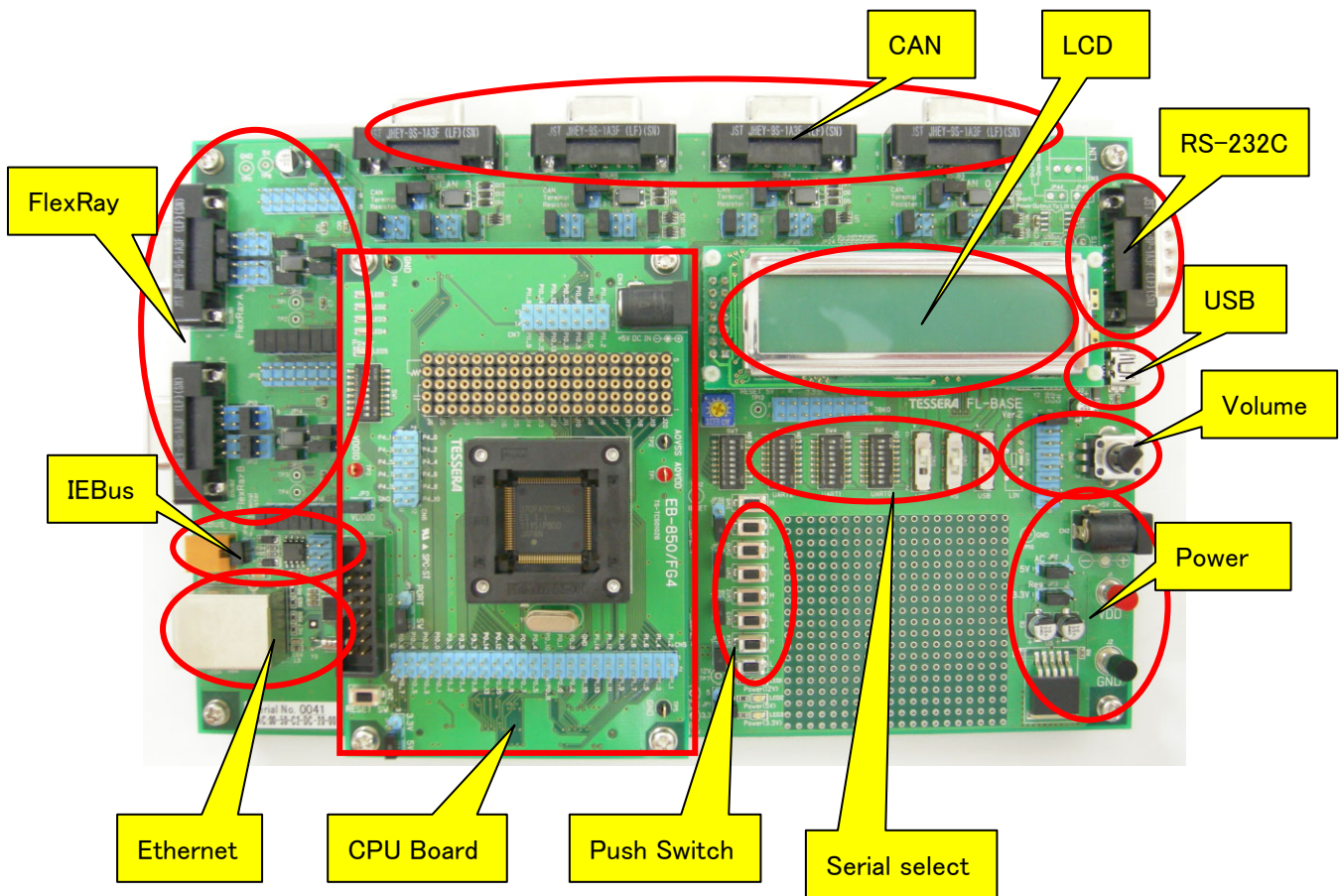
TABLE OF CONTENTS

1	INTRODUCTION	4
2	FEATURES	5
2.1	CAN	6
2.2	FLEXRAY	8
2.3	IEBUS	11
2.4	ETHERNET	12
2.5	SERIAL SELECT	13
2.5.1	<i>LCD</i>	14
2.5.2	<i>RS-232C</i>	17
2.5.3	<i>USB Serial Conversion</i>	18
2.6	PUSH SWITCH	19
2.7	VOLUME.....	20
2.8	POWER	21
2.9	CPU BOARD	22
2.9.1	<i>Power</i>	23
2.9.2	<i>CPU</i>	23
2.9.3	<i>Clock</i>	24
2.9.4	<i>Reset</i>	24
2.9.5	<i>Switch & LED</i>	25
2.9.6	<i>Debug Connector</i>	26
2.9.7	<i>Filter socket</i>	27
3	CPU TERMINAL CONNECTION LIST	28

1 Introduction

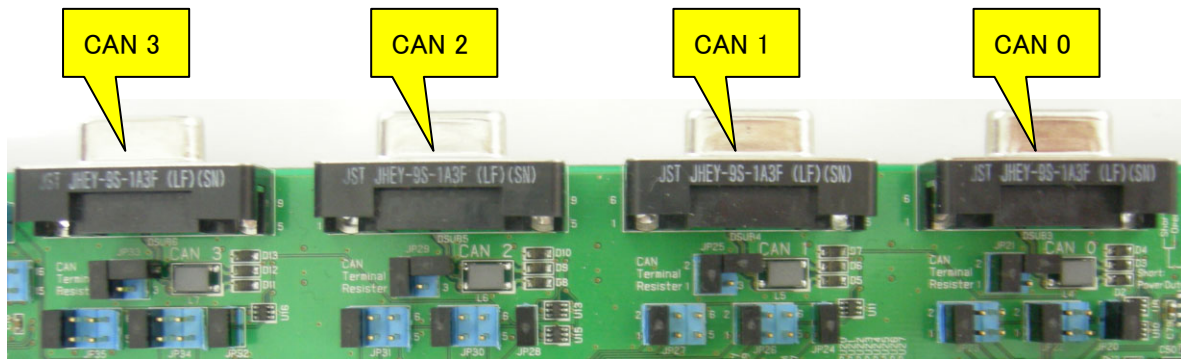
In this document, features and hardware specifications of FL-850/FG4, which the 32-bit single-chip microcomputer V850E2/FG4 from Renesas Electronics Corporation is mounted, are described.

2 Features



2.1 CAN

The CAN controller of the microcomputer is connected to the CAN transceiver (TJA1040). It supports CAN physical layer. Also, CAN bus signal is connected to DSUB 9pin female connector.



One terminal can be selected by using jumpers from maximum of three multipurpose terminals, and can be connected to CAN transceiver.

Only one line must be shorted in each jumper.

Following table shows the connection of V850E2/FG4.

		Jumper		Connector	
P0_4/FCN0TX/INTP11	TxD	JP22	1-2	CAN 0	
P1_1/TAUA0I1/TAUA0O1/ENCA0AIN/FCN1RX/FCN0TX			3-4		
N.C			5-6		
P0_5/FCN0RX/INTP12	RxD	JP23	1-2		
P1_7/TAUA0I7/TAUA0O7/TAPA0WN/FCN0RX/CSIH2CSS1			3-4		
N.C			5-6		
P1_5/TAUA0I5/TAUA0O5/ENCA0TINI/TAPA0VN/CSIH2RY	MODE0	JP20	Short		
P0_7/URTE11RX/FCN1TX/KR0I2/CSIH2CSS2/INTP4	TxD	JP26	1-2		CAN 1
P1_2/TAUA0I2/TAUA0O2/ENCA0BIN/TAPA0UP/CSIH2SI/FCN1TX			3-4		
N.C			5-6		
P0_6/FCN1RX/URTE11TX/KR0I1/CSIH2CSS1/NMI	RxD	JP27	1-2		
P1_1/TAUA0I1/TAUA0O1/ENCA0AIN/FCN1RX/FCN0TX			3-4		
N.C			5-6		
P1_14/TAUA0I14/TAUA0O14/FLX0STPWT/INTP8	MODE1	JP24	Short		
N.C.	TxD	JP30	1-2	CAN 2	
N.C			3-4		
N.C			5-6		
N.C	RxD	JP31	1-2		
N.C			3-4		
N.C			5-6		
N.C.	MODE2	JP28	Short		
N.C.	TxD	JP34	1-2		CAN 3
N.C			3-4		
N.C			5-6		
N.C	RxD	JP35	1-2		
N.C			3-4		
N.C			5-6		
N.C.	MODE3	JP32	Short		

Default

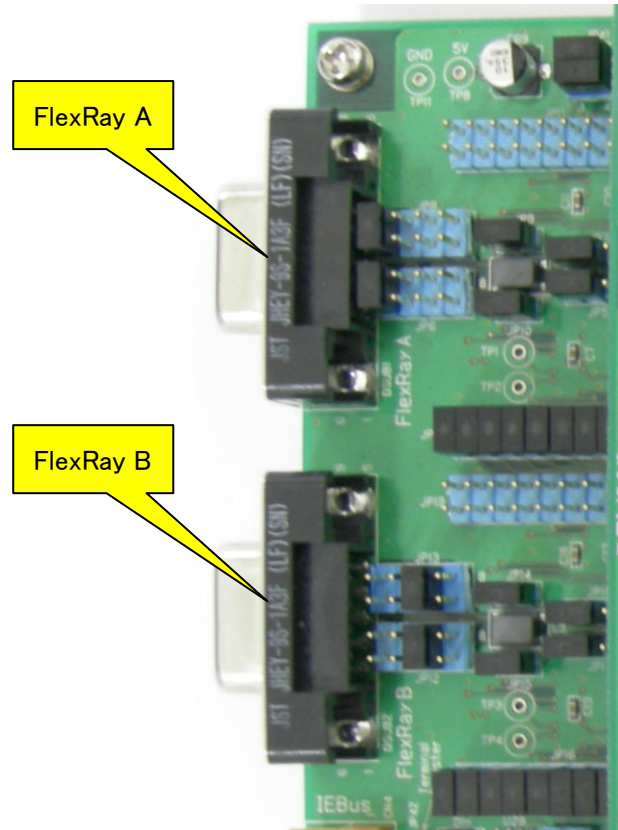
JP21, JP25, JP29, and JP33 are termination resistor connect. Open or short these as needed.

		termination resistor
JP21:CAN 0	1-2 Short 3-4 Short	60 Ω
JP25:CAN 1	1-2 Short 3-4 Open	120 Ω
JP29:CAN 2	1-2 Open 3-4 Open	Non

CAN 0,1,2,3 DSUB Connector	
Pin Number	Signal Name
1	N.C.
2	CANL
3	GND
4	N.C.
5	0.1uF
6	N.C.
7	CANH
8	N.C.
9	N.C.

2.2 FlexRay

The FlexRay controller of the microcomputer is externally connected to the FlexRay transceiver (TJA1080). It supports FlexRay physical layer. Also, FlexRay bus signal is connected to DSUB 9pin female connector.



Following table shows the connections for V850E2/FG4.

	信号名	JP4	TJA1080
P1_11/TAUA0I11/TAUA0O11/URTE3RX/FLX0TXDA/INTP5	FLX0TXDA	1-2	TXD
P1_9/TAUA0I9/TAUA0O9/INTP3/FLX0TXENA/URTE4RX	FLX0TXENA	3-4	TXEN
P3_7/TAUA0I7/TAUA0O7/CSIG0SI/URTE3TX	STBN1	5-6	STBN
P3_4/TAUB0I4/TAUB0O4/KR0I5/CSIG0RY1/CSIG0RYO	EN1	7-8	----
P1_10/TAUA0I10/TAUA0O10/FLX0RXDA/URTE3TX/INTP4	FLX0RXDA	9-10	RXD
P3_5/TAUB0I5/TAUB0O5/KR0I4/CSIG0SC	ERRN1	11-12	ERRN
P3_6/TAUB0I6/TAUB0O6/CSIG0DCS/CSIG0SO	RXEN1	13-14	RXEN
P1_6/TAUA0I6/TAUA0O6/TAPA0WP/_CSIH2SSI/CSIH2CSS0	WAKE1	15-16	WAKE

	信号名	JP16	TJA1080
P1_13/TAUA0I13/TAUA0O13/URTE4RX/FLX0TXDB/INTP7	FLX0TXDB	1-2	TXD
P1_15/TAUA0I15/TAUA0O15/FLX0TXENB/INTP9	FLX0TXENB	3-4	TXEN
P4_8/TAUB1I11/TAUB1O11/CSIG4SC/KR0I0/ENCA0ZIN	STBN2	5-6	STBN
P4_5/TAUB1I7/TAUB1O7/CSIG0SC/KR0I3/ENCA0TIN1	EN2	7-8	----
P1_12/TAUA0I12/TAUA0O12/FLX0RXDB/URTE4TX/INTP6	FLX0RXDB	9-10	RXD
P4_6/TAUB1I9/TAUB1O9/CSIG4SI/URTE11TX/KR0I2/ENCA0AIN	ERRN2	11-12	ERRN
P4_7/INTP4/TAUB1O10/URTE11RX/CSIG4SO/KR0I1/ENCA0BIN	RXEN2	13-14	RXEN
P1_7/TAUA0I7/TAUA0O7/TAPA0WN/FCN0RX/CSIH2CSS1	WAKE2	15-16	WAKE

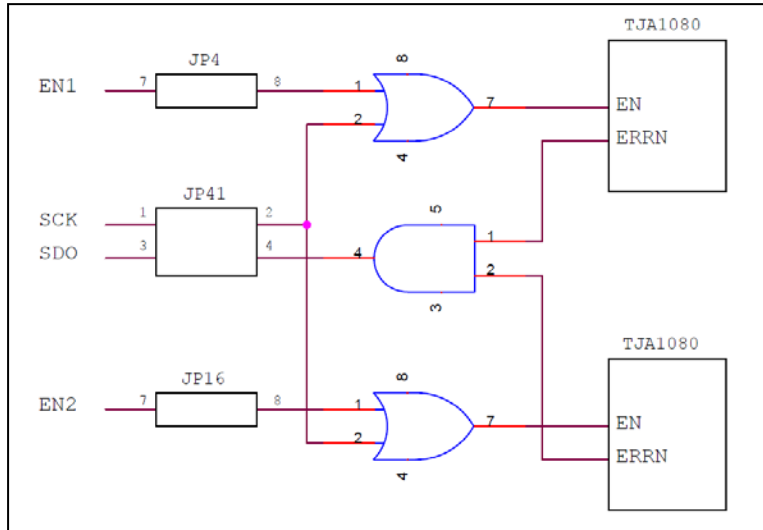
JP11 and JP19 are jumpers for TJA1082 (not mounted). Do not short them.

		JP41
P1_2/TAUA0I2/TAUA0O2/ENCA0BIN/TAPA0UP/CSIH2SI/FCN1 TX	SDO	3-4
P1_4/TAUA0I4/TAUA0O4/ENCA0TIN0/TAPA0VP/CSIH2SC	SCLK	1-2

EN and ERRN terminals of TJA1080 are connected as shown below logic circuit diagram.

Set EN1 terminal to Low when you need to access upper one (FlexRay A) with CSI. Set to High when you do not need to access it.

In the same way, set EN2 terminal to Low when you need to access upper one (FlexRay B) with CSI. Set to High when you do not need to access it.



JP5, JP7, JP17, and JP18 are the selection of FlexRay transceiver IC (TJA1080 or TJA1082).

Normally, use these with the default settings since it does not mount TJA1082.

FlexRay A	JP5 : 1-2 JP7 : 1-2	TJA1080
	JP5 : 2-3 JP7 : 2-3	TJA1082
FlexRay B	JP17 : 1-2 JP18 : 1-2	TJA1080
	JP17 : 2-3 JP18 : 2-3	TJA1082

JP9, JP10, JP14, and JP15 are the connection for termination resistor (50 Ω). Open or short these as needed.

FlexRay A	JP9	BP
	JP10	BM
FlexRay B	JP14	BP
	JP15	BM

Default: Short

JP6, JP8, JP12, and JP13 are the jumpers to change wire connection of DSUB 9pin female connector, which outputs FlexRay bus signal.

Type-1

JP6	1-2
JP8	1-2
JP12	5-6
JP13	5-6

FlexRay A DSUB connector		FlexRay B DSUB connector	
Pin No.	Signal	Pin No.	Signal
1	N.C.	1	N.C.
2	BM A	2	BM B
3	N.C.	3	N.C.
4	N.C.	4	N.C.
5	N.C.	5	N.C.
6	N.C.	6	N.C.
7	BP A	7	BP B
8	N.C.	8	N.C.
9	N.C.	9	N.C.

Type-2

JP6	1-2
JP8	1-2
JP12	3-4
JP13	3-4

FlexRay A DSUB connector		FlexRay B DSUB connector	
Pin No.	Signal	Pin No.	Signal
1	N.C.	1	N.C.
2	BM A	2	N.C.
3	BM B	3	N.C.
4	N.C.	4	N.C.
5	N.C.	5	N.C.
6	N.C.	6	N.C.
7	BP A	7	N.C.
8	BP B	8	N.C.
9	N.C.	9	N.C.

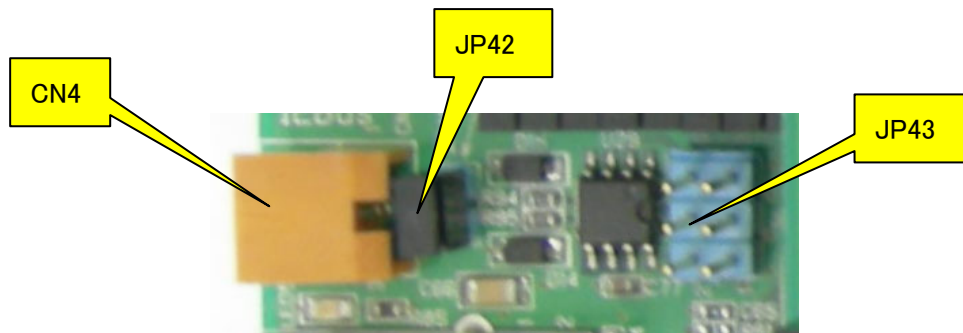
Type-3

JP6	1-2 5-6
JP8	1-2 5-6
JP12	All Open
JP13	All Open

FlexRay A DSUB connector		FlexRay B DSUB connector	
Pin No.	Signal	Pin No.	Signal
1	N.C.	1	N.C.
2	BM A	2	BM A
3	N.C.	3	N.C.
4	N.C.	4	N.C.
5	N.C.	5	N.C.
6	N.C.	6	N.C.
7	BP A	7	BP A
8	N.C.	8	N.C.
9	N.C.	9	N.C.

2.3 IEBus

V850E2/FG4 does not have IEBus controller, therefore it cannot use IEBus.

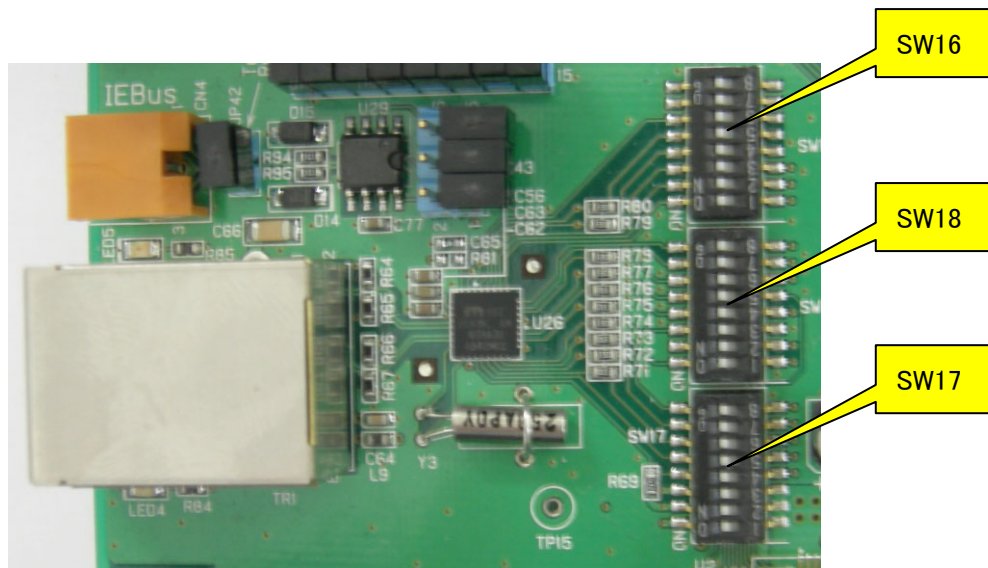


Default Settings JP43: Open
 JP42: Short

CN4 Pin Number	Function Name
1	(+) Bus Output, (+) Receiver Input
2	GND
3	(-) Bus Output, (-) Receiver Input

2.4 Ethernet

V850E2/FG4 does not have MAC controller, therefore it cannot use Ethernet.



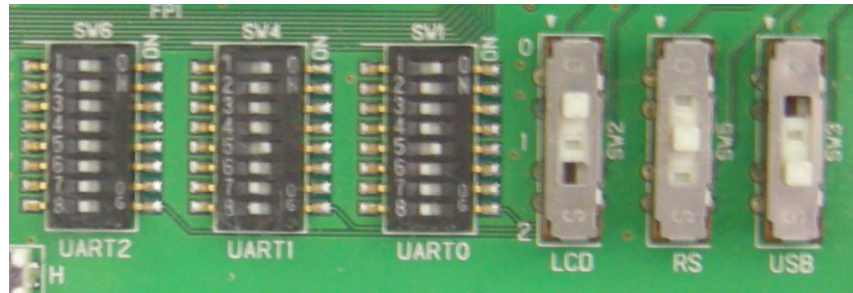
The function of Ethernet is not used, and make the following dip switches all turning off.

There is a possibility of breaking when turning it on.

- SW16 (Default OFF)
- SW17 (Default OFF)
- SW18 (Default OFF)

2.5 Serial select

It can be connected by selecting the microcomputer's UART terminal to "LCD", "RS-232C", and "USB Serial Conversion".



The terminals for using UART can be selected by DIP switch (SW1, SW4, and SW6).

※ Do not set multiple ON within a group.

		SW1		
P0_8/URTE10TX/KR0I3/CSIH2CSS3/INTP5/TAUA005/IICB0SDA	TXD	1	ON	UART0
P4_3/TAUB1I5/TAUB1O5/CSIG0SI/URTE10TX		2	OFF	
P1_10/TAUA0I10/TAUA0010/FLX0RXDA/URTE3TX/INTP4		3	OFF	
	N.C.	4	OFF	
P0_9/URTE10RX/KR0I4/CSIH2CSS4/INTP6/TAUA006/IICB0SCL	RXD	5	ON	
P4_4/INTP2/TAUB1O6/URTE10RX/CSIG0SO/ENCA0TIN0		6	OFF	
P1_11/TAUA0I11/TAUA0011/URTE3RX/FLX0TXDA/INTP5		7	OFF	
	N.C.	8	OFF	

		SW4		
P4_2/TAUB1I3/TAUB1O3/TAUA0I15/TAUA0015/URTE2TX	TXD	1	ON	UART1
P1_8/TAUA0I8/TAUA008/URTE4TX		2	OFF	
P1_12/TAUA0I12/TAUA0012/FLX0RXDB/URTE4TX/INTP6		3	OFF	
	N.C.	4	OFF	
P4_1/TAUB1I2/TAUB1O2/TAUA0I14/TAUA0014/URTE2RX	RXD	5	ON	
P1_9/TAUA0I9/TAUA009/INTP3/FLX0TXENA/URTE4RX		6	OFF	
P1_13/TAUA0I13/TAUA0013/URTE4RX/FLX0TXDB/INTP7		7	OFF	
	N.C.	8	OFF	

		SW6		
N.C.	TXD	1	OFF	UART2
P0_6/FCN1RX/URTE11TX/KR0I1/CSIH2CSS1/NMI		2	OFF	
P4_6/TAUB1I9/TAUB1O9/CSIG4SI/URTE11TX/KR0I2/ENCA0AIN		3	OFF	
	N.C.	4	OFF	
N.C.	RXD	5	OFF	
P0_7/URTE11RX/FCN1TX/KR0I2/CSIH2CSS2/INTP4		6	OFF	
P4_7/INTP4/TAUB1O10/URTE11RX/CSIG4SO/KR0I1/ENCA0BIN		7	OFF	
	N.C.	8	OFF	

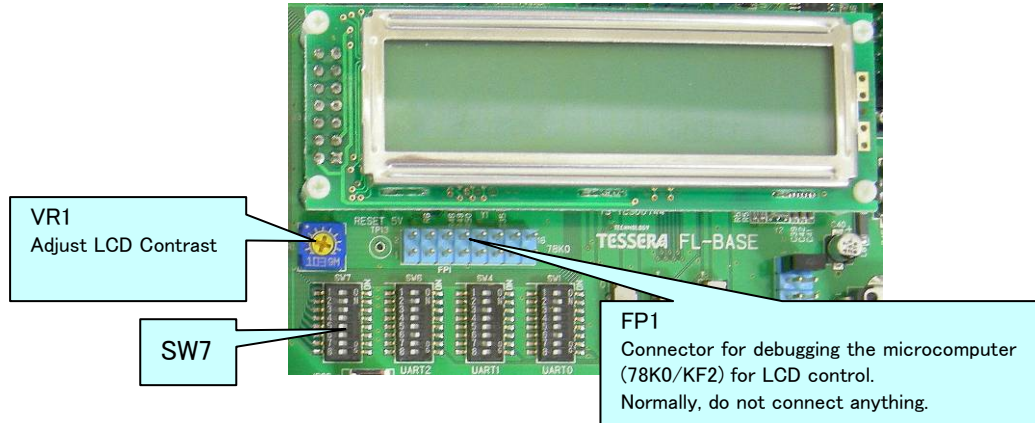
The destination for UART can be selected by the slide switch (SW2, SW3, and SW5).

	Slide Switch	
SW2 LCD	0	UART0
	1	UART1
	2	UART2
SW5 RS-232C	0	UART0
	1	UART1
	2	UART2
SW3 USB Serial Conversion	0	UART0
	1	UART1
	2	UART2

2.5.1 LCD

Words can be displayed on LCD panel by sending data to UART that is connected to LCD. "Binary mode" to display hexadecimal and "ASCII mode" to display ASCII characters can be selected by the DIP switch (SW7).

Initial screen displays when you press the reset switch on CPU board.



UART Communication Specifications

- Baud Rate 115.2Kbps (Fixed)
- Data Length 8bit (LSB First)
- Parity None
- Stop Bit 1bit
- Flow Control None (continuous transmission enabled)

Binary Mode 1 (SW7-1:ON, SW7-2:ON, SW7-3:Any)

It displays the hexadecimal data as sent with entering space between 1Byte data.

It can display 10Byte in 1 screen. It scrolls 1 line when it received 11Byte of data.

(example) `URTH?TX = 0x01; TXWait();`

`URTH?TX = 0x02; TXWait();`

.....

`URTH?TX = 0x0A; TXWait();`

↪

0	1		0	2		0	3		0	4		0	5		
0	6		0	7		0	8		0	9		0	A		

`URTH?TX = 0x10; TXWait();`

↪

0	6		0	7		0	8		0	9		0	A		
1	0														

(use case) By developing a program to send 10Byte once in 1 second, it will display the first 1Byte at the top-left of the screen.

Binary Mode 2 (SW7-1:ON, SW7-2:OFF, SW7-3:ON)

It displays the hexadecimal data as sent without entering space between 1Byte data.

It can display 16Byte in 1 screen. It scrolls 1 line when it received 17Byte of data.

(example) URTH?TX = 0x01; TXWait();

URTH?TX = 0x02; TXWait();

.....

URTH?TX = 0x10; TXWait();



0	1	0	2	0	3	0	4	0	5	0	6	0	7	0	8
0	9	0	A	0	B	0	C	0	D	0	E	0	F	1	0

URTH?TX = 0x11; TXWait();



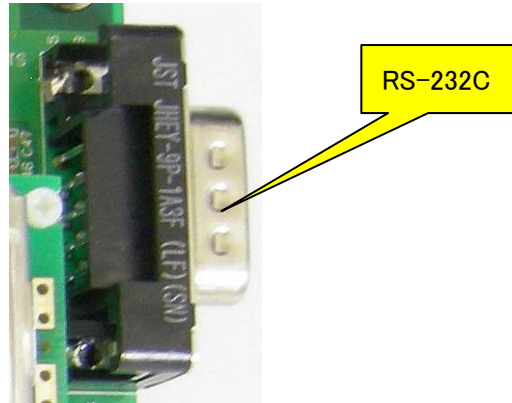
0	9	0	A	0	B	0	C	0	D	0	E	0	F	1	0
1	1														

(use case) By developing a program to send 16Byte once in 1 second, it will display the first 1Byte at the top-left of the screen.

2. 5. 2 RS-232C

UART that is connected to "RS-232C" can send and receive signals with the RS-232C level of D-SUB9 pin connector.

Use a cross cable when you connect to PC.

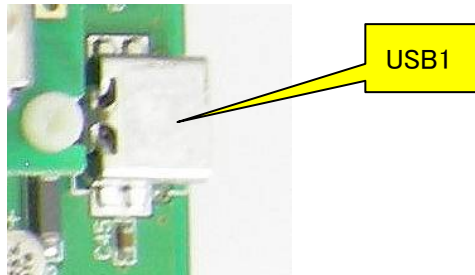


RS-232C D-SUB Connector	
Pin Number	Signal
1	N.C.
2	RxD
3	TxD
4	N.C.
5	GND
6	N.C.
7	RTS(N.C.)
8	CTS(N.C.)
9	N.C.

2.5.3 USB Serial Conversion

UART that is connected to "USB serial conversion" can communicate with the COM port of PC through USB microcomputer (uPD78F0730).

USB driver is stored in the same media as this manual. When you encountered a warning "Windows Logo Test" while installing the USB driver, please select "Continue".



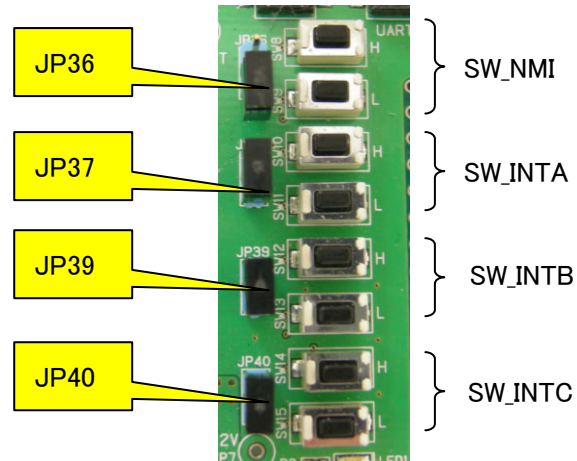
Recommended UART communication specification

- Baud rate 115.2Kbps
- Data length 8bit (LSB First)
- Parity None
- Stop Bit 1bit
- Flow Control None

2.6 Push Switch

4 interrupt signals can be connected to microcomputer's interrupt terminals. The signal can be set to High by pressing H button, and to Low by pressing L button. It becomes High by reset signal of the CPU.

Also, it has chattering prevention circuit.

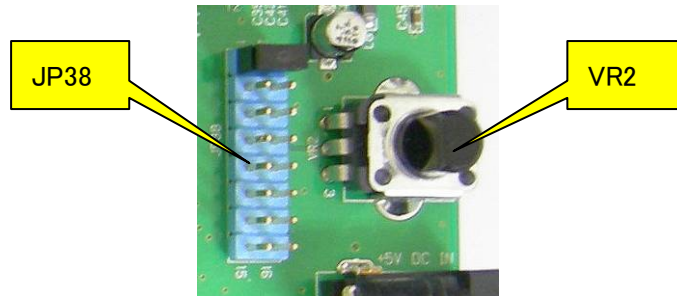


The interrupt signals are disconnected by taking each jumper pin out.

	Jumper	Switch	Signal
P0_6/FCN1RX/URTE11TX/KR01I/CSIH2CSS1/ NMI	JP36: Open	SW8/9	SW_NMI
P0_3/TAUJ1I3/TAUJ1O3/CSIG4SC/ADCA0TRG1/ INTP3 /TAPA0ESO/MODE1	JP37: Short	SW10/11	SW_INTA
P0_13/TAUJ0I1/TAUJ0O1/KR0I5/CSIH2CSS5/ INTP7 /CSIG0SI	JP39: Short	SW12/13	SW_INTB
P0_12/TAUJ0I0/TAUJ0O0/KR0I0/ INTP8 /CSIG0SSI/CSCXFOUT	JP40: Short	SW14/15	SW_INTC

2.7 Volume

It can output variable voltage (0V-IO voltage) to A/D terminal of CPU by variable resistor of 10KΩ.

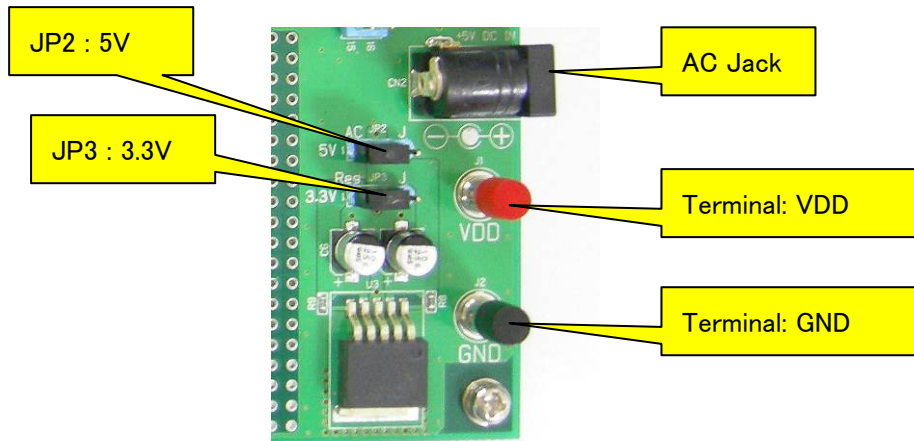


	JP38
ADCA010	1-2
ADCA011	3-4
ADCA012	5-6
ADCA013	7-8
ADCA014	9-10
ADCA015	11-12
P10_6/ADCA016	13-14
P10_7/ADCA017	15-16

2.8 Power

Connect bundled AC adapter (+5V) to AC Jack. You do not need to connect to the AC Jack on the GPU board.

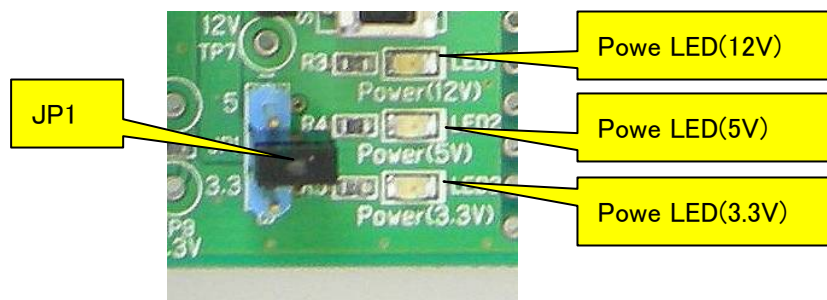
It generates the power of +12V for FlexRay driver and +3.3V for Ethernet PHY chip power from this power supply with using regulator.



Power supply source can be changed by JP2 and JP3.

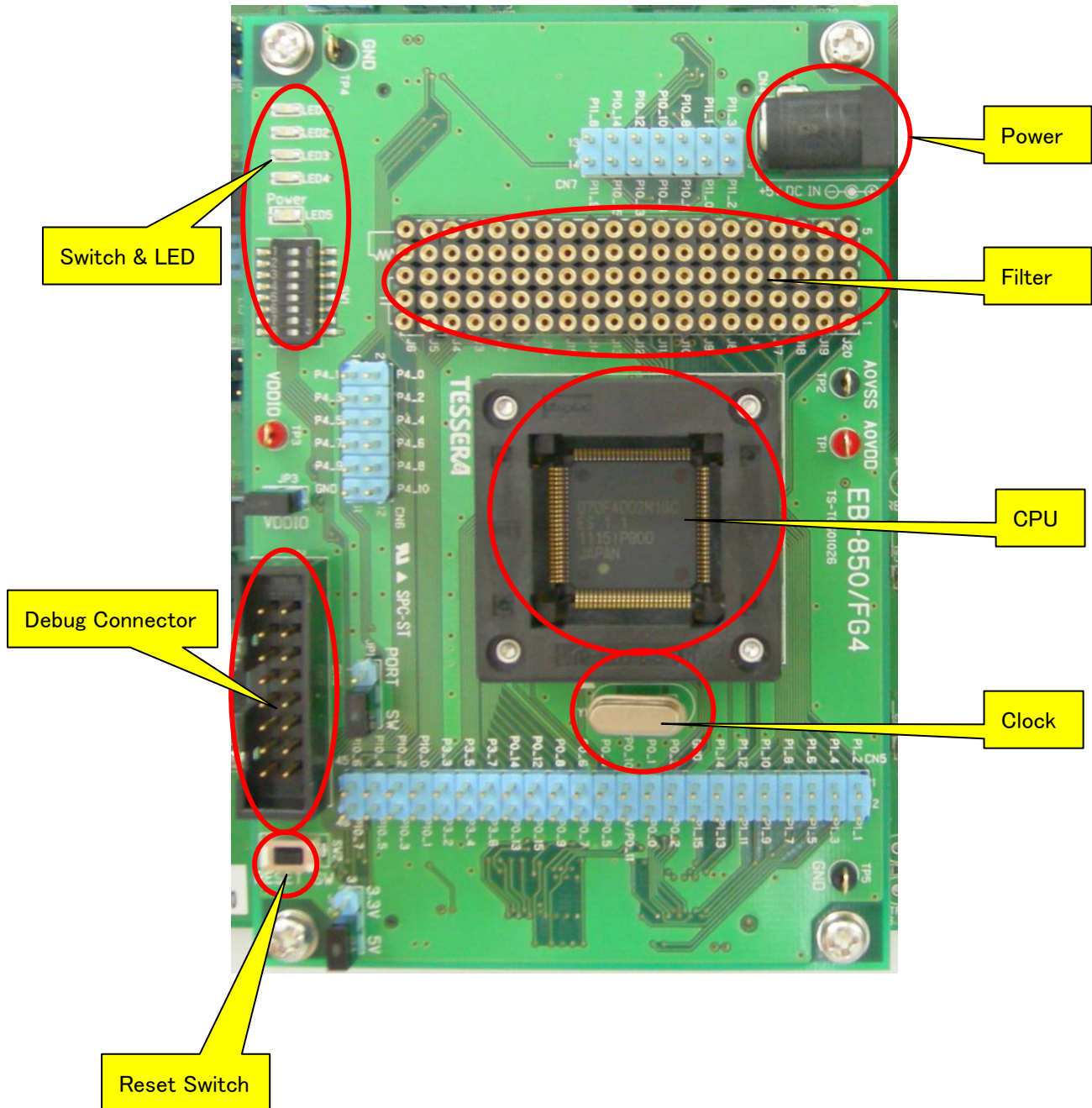
JP2	1-2	AC adapter
5V	2-3	Terminal
JP3	1-2	Regulator
3.3V	2-3	Terminal

JP1 is the jumper to fix the IO voltage when it does not connect CPU board. Normally, do not short this.



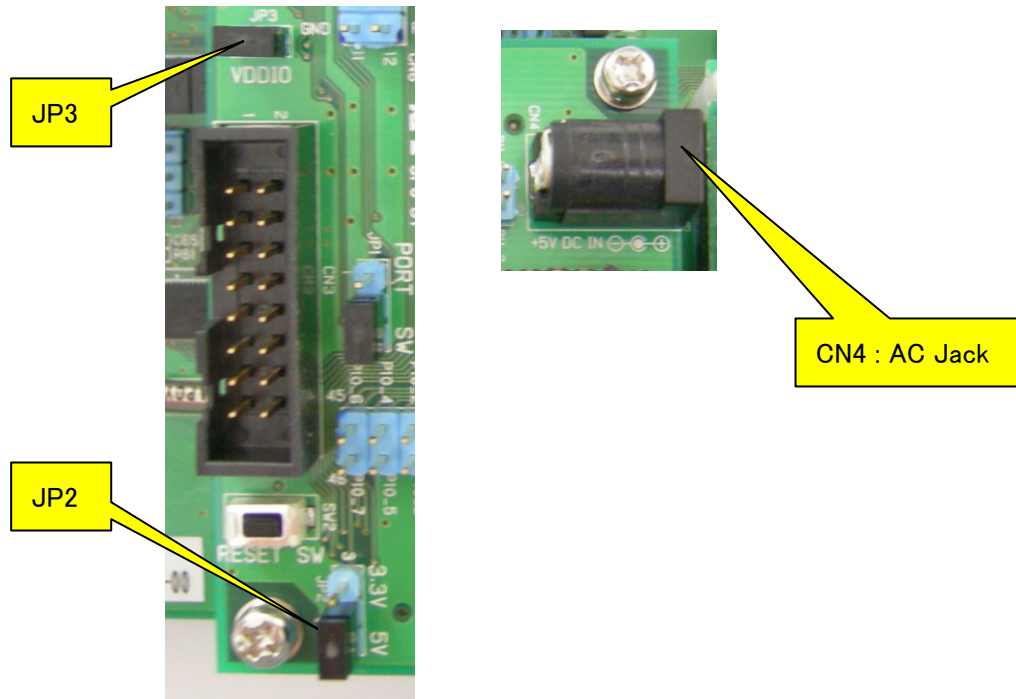
2.9 CPU Board

One of "EB-850/FG4" or "EB-850/FG4-S" is mounted on the CPU board



2.9.1 Power

There is a jumper pin for measuring the current when you use only CPU board itself.

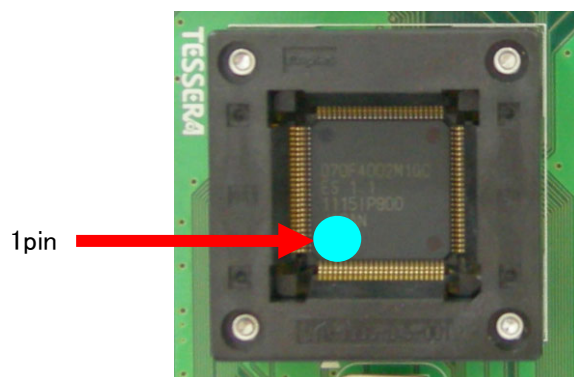


JP3	Connect ammeter to check the current	
JP2	1-2	Operation voltage is 5V.
	2-3	Operation voltage is 3.3V. (Only when FL-BASE board is connected)

2.9.2 CPU

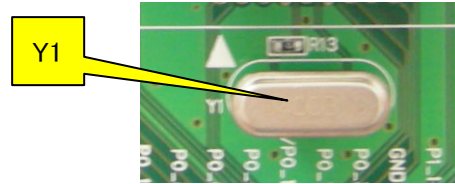
CPU is direct-mounted for "EB-850/FG4".

For "EB-850/FG4-S", only socket is mounted. Make sure the position of 1pin when you mount CPU.



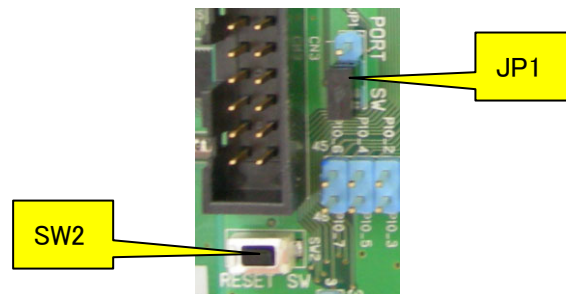
2.9.3 Clock

For the X1 and X2 of the CPU, **4MHz** crystal oscillator (Y1) is mounted on the socket.



2.9.4 Reset

CPU can be reset by pressing the Reset switch (SW2).

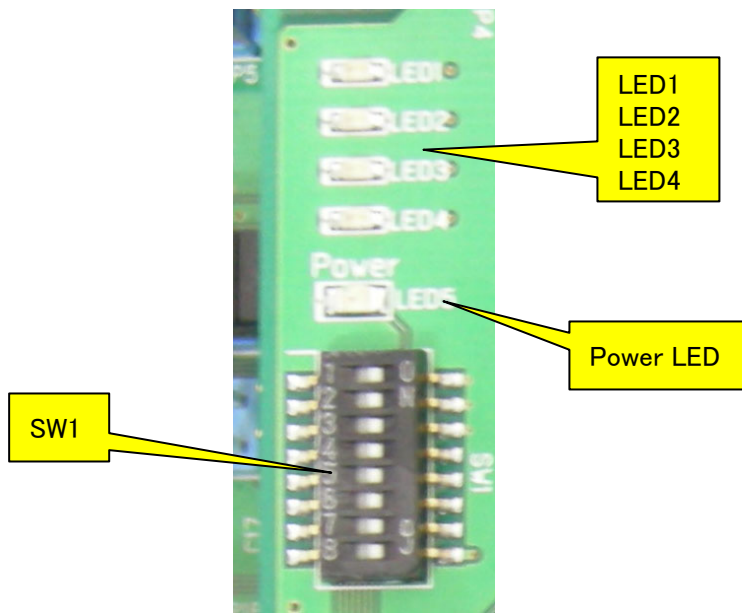


The method of outputting reset on the FL-BASE board can be set with the jumper.

No.	Select	Note
JP1	1-2	CPU Port(P0_0)
	2-3	Reset Switch(SW2)

2.9.5 Switch & LED

They are connected to port terminals of the CPU.

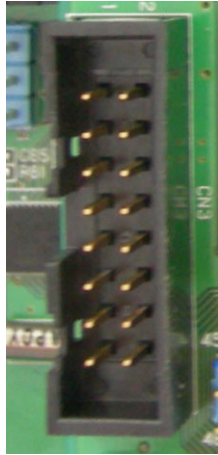


- P0_2, P0_14, and P0_15 can be used for the switch inputs.
It connects the pull-up resistor with built-in CPU. Set the switch to OFF to read High and to ON to read Low.
- P3_2, P3_3, P4_9, and P4_10 can be connected to LED. Set the switch ON and output Low from the port to light the LED.
- SW1-8 is power indicator. Power LED is off when power is OFF.

	SW1	Connect to
P0_2/TAUJ1I2/TAUJ1O2/CSIG4SI/ADCA0TRG2/URTE2TX/INTP2/TAUA0O2/MODE0	1	GND
P0_14/TAUJ0I2/TAUJ0O2/KR0I6/CSIH2CSS6/TAUB1O13/CSIG0DCS/CSIG0SO	2	GND
P0_15/TAUJ0I3/TAUJ0O3/KR0I7/CSIH2CSS7/TAUB1O14/CSIG0SC	3	GND
P3_2/TAUB0I2/TAUB0O2/KR0I7	4	LED1
P3_3/TAUB0I3/TAUB0O3/KR0I6	5	LED2
P4_9/TAUB1I13/TAUB1O13/CSIG0RYO	6	LED3
P4_10/TAUB1I14/TAUB1O14/CSIG4RYI	7	LED4
5V Power Supply	8	Power LED

2.9.6 Debug Connector

Debugger or Flash writer can be connected to CN4.



It supports "QB-V850MINIL" and "E1" emulator.

Please use the 16pin conversion adaptor of the "QB-V850MINIL" attachment when you connect "QB-V850MINIL".

Please use the 14pin conversion adaptor "E1-16C" of this product attachment when you connect "E1".

For the Flash writer, it supports "PG-FP5" writer.

CN4

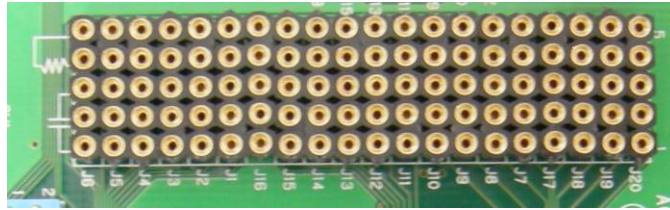
Pin Number	Signal		
	Debugger	Writer	
1	GND	←	←
2	RESET	←	←
3	DCUTDO	SO	
4	VDD	←	←
5	DCUTDI	SI	RxD/TxD
6	N.C.		
7	DCUTCK	SCK	
8	DCUTRDY		
9	DCUTRST		
10	N.C.		
11	N.C.		
12	DCUTMS		
13	N.C.		
14	FLMD0	←	←
15	T_RESET		
16	N.C.		

E1-16C

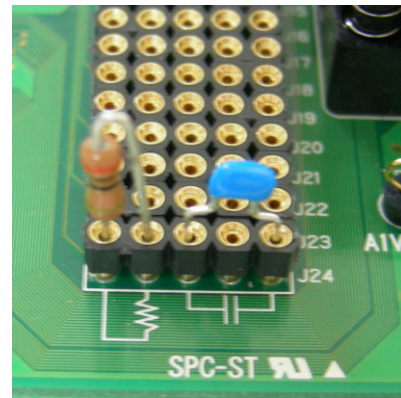
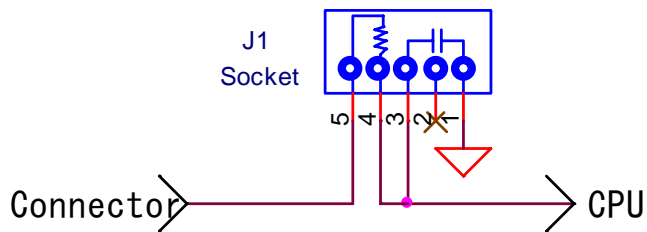
Pin Number	Signal
1	DCUTCK
2	GND
3	DCUTRST
4	FLMD0
5	DCUTDO
6	T_RESET
7	DCUTDI
8	VDD
9	DCUTMS
10	RESET
11	DCUTRDY
12	GND
13	RESET
14	GND

2.9.7 Filter socket

Filters can be implemented to A/D input terminals.



Connects (CN1, CN2) are connected through the sockets as illustrated below. Therefore, please make sure you connect resistor between the socket 4pin and 5pin when you use A/D terminal.



	Socket
ADCA0I0	J1
ADCA0I1	J2
ADCA0I2	J3
ADCA0I3	J4
ADCA0I4	J5
ADCA0I5	J6
P10_6/ADCA0I6	J7
P10_7/ADCA0I7	J8
P10_8/ADCA0I8	J9
P10_9/ADCA0I9/ADCA0TRG0	J10

	Socket
P10_10/ADCA0I10/ADCA0TRG1	J11
P10_11/ADCA0I11/ADCA0TRG2	J12
P10_12/ADCA0I12	J13
P10_13/ADCA0I13	J14
P10_14/ADCA0I14	J15
P10_15/ADCA0I15	J16
P11_0/ADCA0I16	J17
P11_1/ADCA0I17	J18
P11_2/ADCA0I18	J19
P11_3/ADCA0I19	J20

3 CPU Terminal Connection List

Please refer to the Excel file which separately distributed.