CEB-V850ES/FJ3·SJ3 EVALUATION BOARD HARDWARE USER'S MANUAL

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CONTENTS

1. Overview

This manual prescribes a CEB-V850ES/FJ3 evaluation board and a CEB-V850ES/SJ3 evaluation board. CEB-V850ES/FJ3·SJ3 is called below about two kinds of evaluation boards.

2. Evaluation CPU Board CEB-V850ES/FJ3·SJ3

The CEB-V850ES/FJ3 features an NEC Electronics-made 32-bit single-chip microcontroller V850ES/FJ3, USB interface, 7-segment LED, CAN interface, LIN interface, N-wire connector, etc.
The CEB-V850ES/SJ3 features an NEC Electronics-made 32-bit single-chip microcontroller V850ES/SJ3. Other devices are the same as CEB-V850-ES/FJ3.
This board is designed so that the CPU pins can be provided outside the board by connecting an optional add-in board.
The MINICUBE or the MINICUBE2 can be used as debugging environment.
The FL-PR4 (FlashPro4) (hereafter, FL-PR4) made by Naito Densei Machida Mfg. Co., Ltd. is required for writing programs. *Besides FL-PR4, FP-LITE and MINICUBE2 can be written in.
The MINICUBE, the MINICUBE2, the FL-PR4 are not included with this evaluation kit.

3. Document

The following documents are included as PDF files.

CEB-V850ES/FJ3·SJ3 Evaluation Board Hardware User's Manual
CEB-V850ES/FJ3 Evaluation Board Circuit Diagrams
CEB-V850ES/FJ3 Evaluation Board Parts List
CEB-V850ES/SJ3 Evaluation Board Circuit Diagrams
CEB-V850ES/SJ3 Evaluation Board Parts List
V850ES/FJ3 Hardware Preliminary User's Manual
V850ES/SJ3 Hardware Preliminary User's Manual

4.1 Hardware Specifications

The specifications of the CEB-V850ES/FJ3·SJ3 Starter's Kit Evaluation Board are shown below.

• CPU	V850ES/FJ3 × 1 (or V850ES/SJ3) ·V850ES/FJ3 Operating CLK direct mode: 6 MHz, PLL mode: 48 MHz Oscillator (MAIN: 6 MHz , SUB: 32.768 KHz) ·V850ES/SJ3 Operating CLK direct mode: 4 MHz, PLL mode: 32 MHz Oscillator (MAIN: 4 MHz , SUB: 32.768 KHz) * The crystal for MAIN clocks is socket-mounted.
• Check pin	A through hole for each signal line check is around CPU. (Two rows of half pitch)
• External connectors	Expansion connector (30-pin 2.54 pitch) × 2 Flash PRO4 connector (16-pin) × 1 MINICUBE connector (26-pin) × 1 CAN-I/F connector (9-pin D-SUB [female]) × 2 LIN-I/F connector (3-pin) × 2
• SW	PUSH SW × 3 (RESET, NMI, INT0) DIP SW (8-bit) × 1
• Jumpers	Development environment setting(FL-PR4·MINICUBE/MINICUBE2) UART setting (USB/FL-PR4·MINICUBE2) CAN termination resistance setting LIN-master/slave switching
• LED	Power LED (+5 V): Green, 7-segment LED × **1**
• Check pin	+12 V, +5 V, +3.3 V, GND
• Power supply	AC adapter (DC+12 V) input With regulator IC, +5 V(FJ3) , +3.3V(SJ3) output

4.2 Block Diagram

Whole block diagram

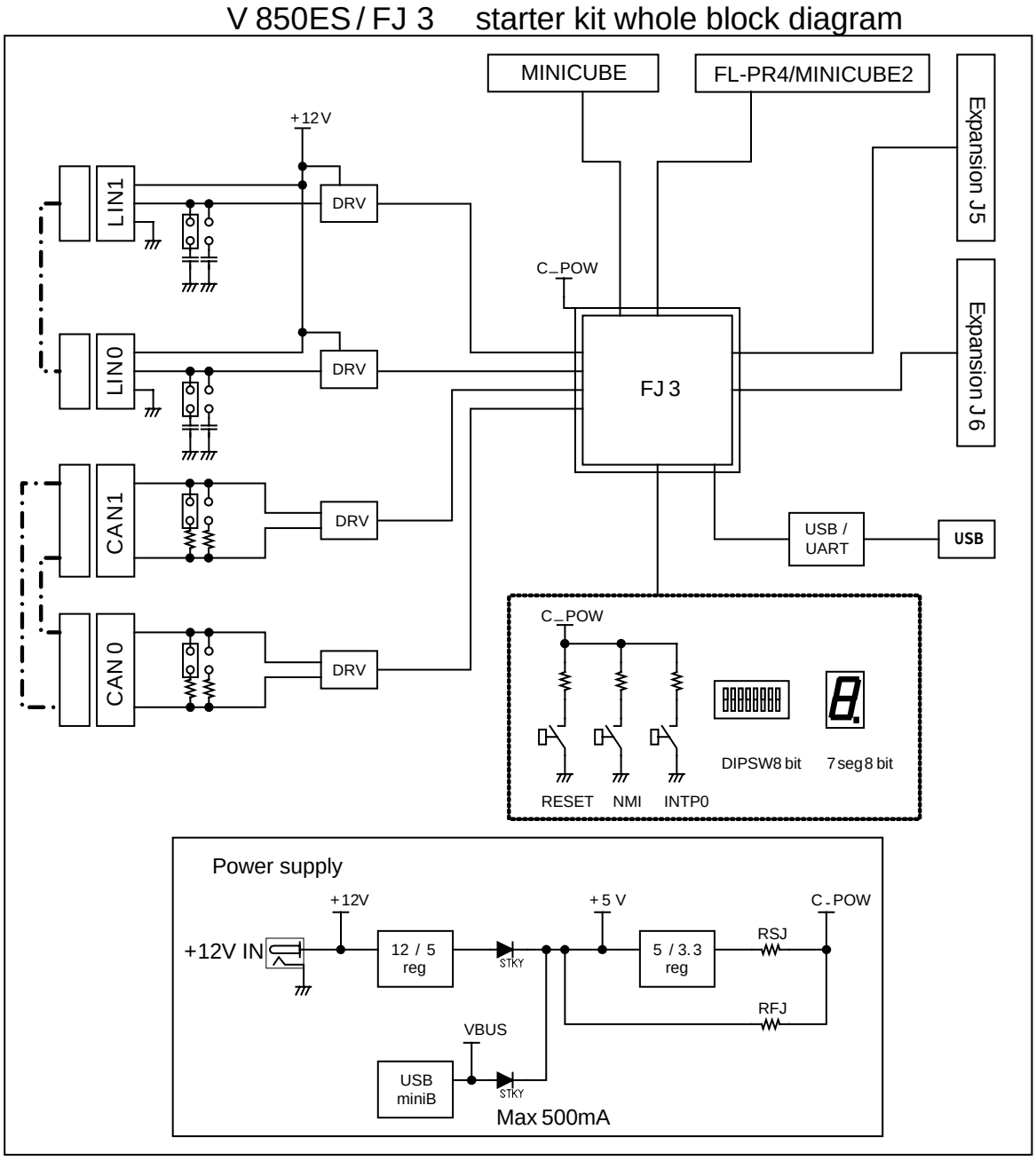


Figure 4.2

The above figure is the case where V850ES/FJ3 is mounted. In this case, CPU power supply voltage is set to +5V. Moreover, when V850ES/SJ3 is mounted, CPU power supply voltage is set to +3.3V.*

* Since a voltage setup is set up at the time of shipment, especially a visitor does not need to be conscious of it.

4.3 Configuration

The following figure shows the physical placement and the outside of the major components on the CEB-V850ES/FJ3·SJ3 evaluation CPU board.
The various components are described below.

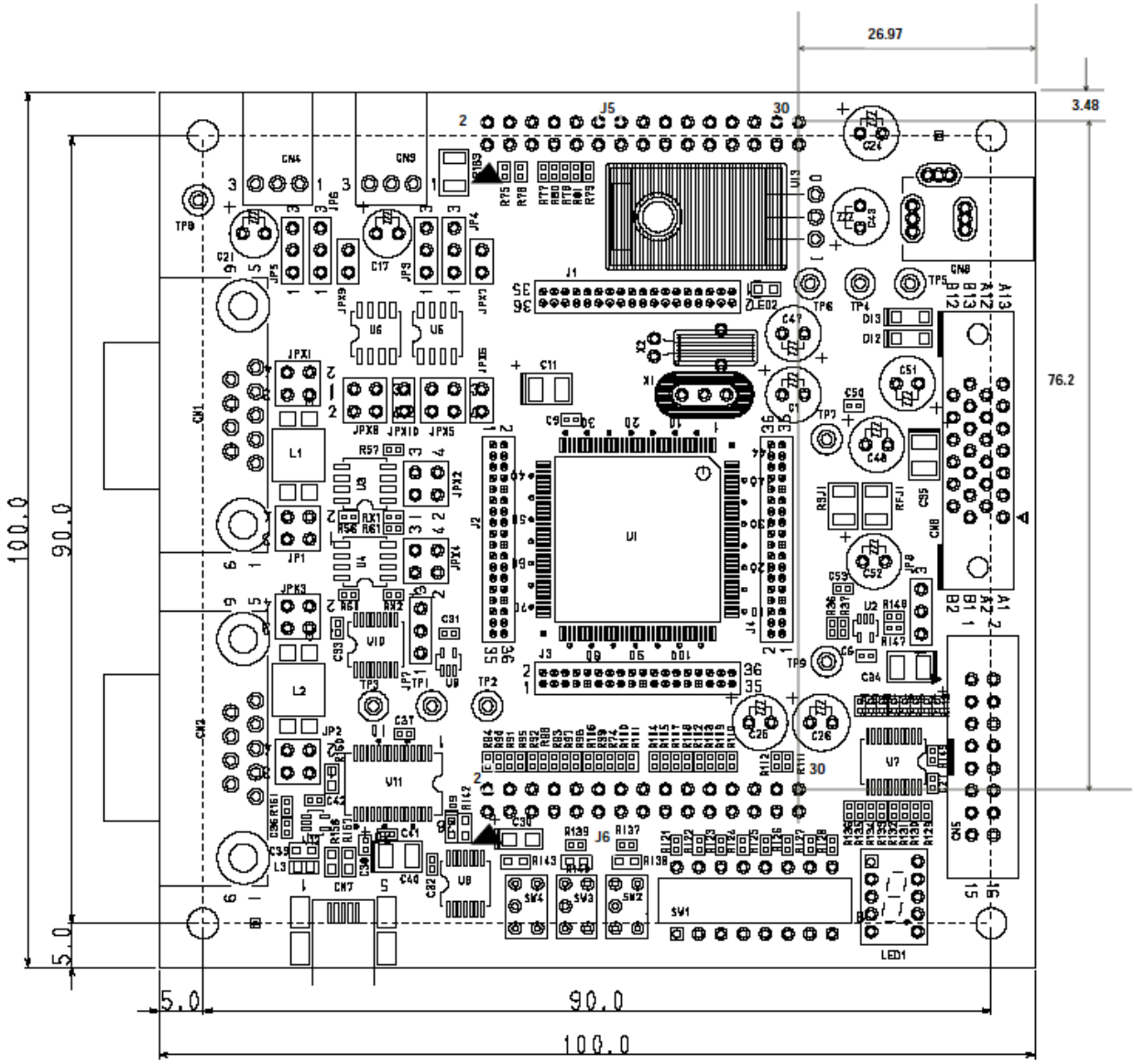


Figure 4.3

4.3.1 Power supply

(1) Power supply part

Although premised fundamental on use in +12V input from the attached AC/DC adaptor, it is possible to also make it operate by the power supply supply from a USB port.

Notes: As for the USB port, power supply supply capability is restricted to 500mA by specification. When you operate this board in a USB port, please use consumption current by 500mA or less. moreover, since +5V are supplied from a USB port, A LIN-I/F function cannot be used.

A block diagram is shown below.

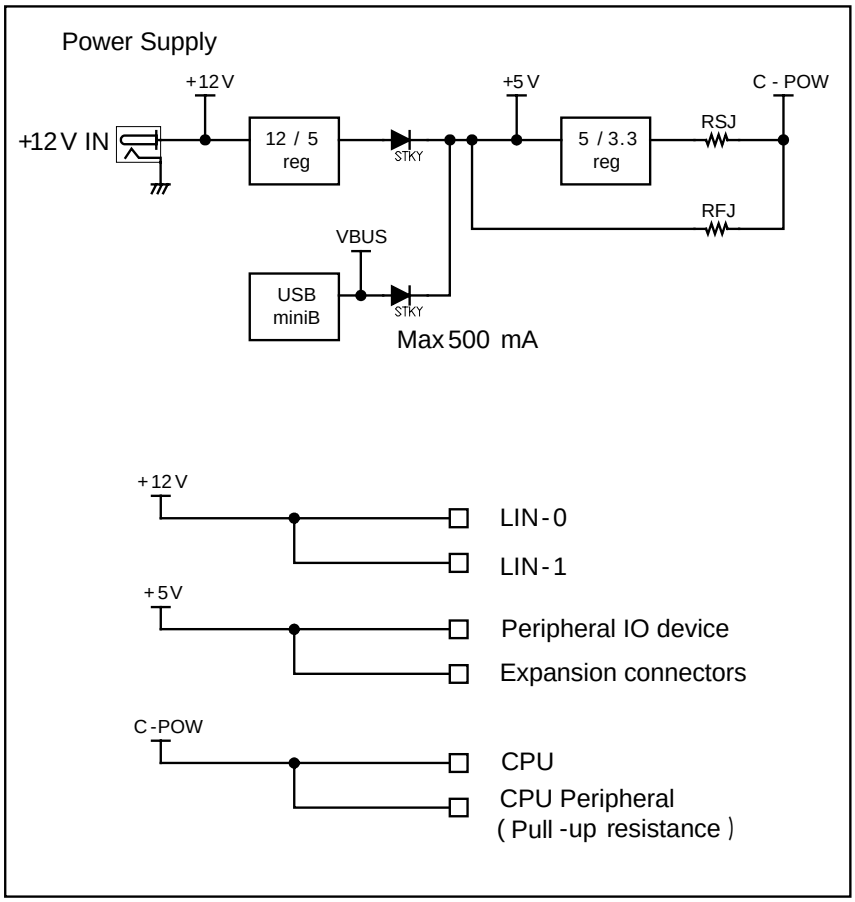


Figure 4.3.1 (1)

(2) Power supply connector (CN8)

Please use DC jack side of an attached AC adaptor for a power supply connector (CN8), connecting. The power supply to supply is as follows.

AC adaptor : NP12-US1210 (Akizuki Denshi Corp)
Input voltage range : 100-240 V 50/60 Hz
Output voltage : DC12 V
Current : 1 A max
Suitable connector : Type A (ϕ5.5)
Polarity :

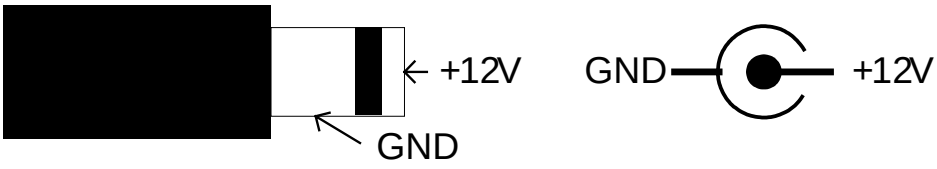


Figure 4.3.1 (2)

4.3.2 CAN-I/F

(1) CAN-I/F overview

Two CAN interfaces are mounted as standard.

A block diagram is shown below.

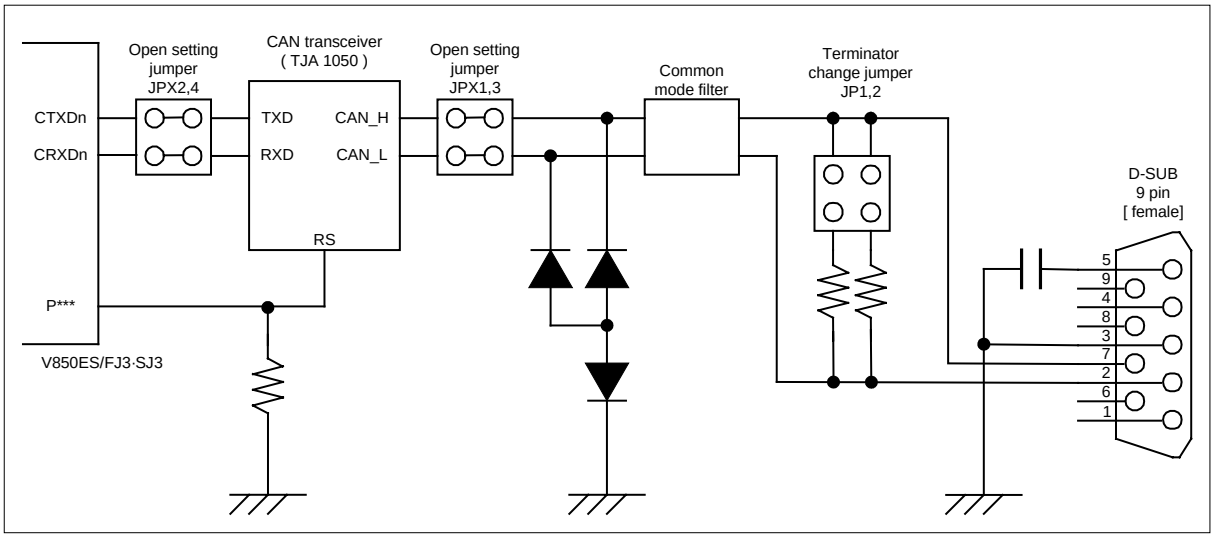


Figure 4.3.2 (1)

(2) CAN-I/F connector (CN1, CN2)

CAN0 is assigned to CN1 and CAN1 is assigned to CN2, respectively.

Since the connector on a substrate mounts Dsub9 pin (female), the connector by the side of a cable should use Dsub9 pin (male) at the time of cable creation.

Pin distribution table is shown below.

CAN I/F connector pin distribution table

Pin№	CN1(CAN0)	CN2(CAN1)
1	N.C.	N.C.
2	CAN_L1	CAN_L2
3	GND	GND
4	N.C.	N.C.
5	Coupling with capacitor and fed to GND.	Coupling with capacitor and fed to GND.
6	N.C.	N.C.
7	CAN_H1	CAN_H2
8	N.C.	N.C.
9	N.C.	N.C.

Table 4.3.2 (2)

Connector part number : XM3B-0922-112 (OMRON Corp.)

(3) CAN transceiver

TJA1050T (made by Philips Corp.) are mounted in this board as a CAN transceiver.
Refer to the applicable data sheet for the details of a device.
Connection of CPU and a CAN transceiver is shown below.

CAN0 connection

CPU	TJA1050T	Signal Name
CTXD0（P33）	TXD	Transmitting data
CRXD0（P34）	RXD	Receiving data
	VREF	VREF
	CAN_H,CAN_L	CAN
PCM4	RS	RS
	VCC,GND	Power supply（+5Vsupply）

Table 4.3.2 (3)-1

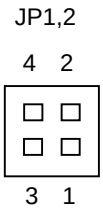
CAN1 connection

CPU	TJA1050T	Signal Name
CTXD1（P36）	TXD	Transmitting data
CRXD1（P37）	RXD	Receiving data
	VREF	VREF
	CAN_H,CAN_L	CAN
PCM5	RS	RS
	VCC,GND	Power supply(+5Vsupply)

Table 4.3.2 (3)-2

(4) CAN signal terminus setup

A CAN signal terminus value is set up by JP1 and JP2.
JP1 corresponds to CAN0 and JP2 correspond to CAN1, respectively.



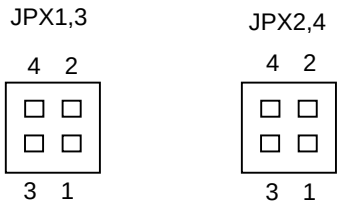
Setup	Terminator value (common to JP1 and JP2)
open	Infinite (default)
1-2 short circuit	120Ω
1-2,3-4 short circuit	60Ω
others	Prohibition of a setup

Table 4.3.2 (4)

(5) About JPX1-JPX4

Although the pattern connects between 1-2 and between 3-4 of JPX1-JPX4, a signal is separable by cutting the pattern on the back side (soldering side) of each jumper.

As standard, the following jumper is un-mounting.



The installation part of each jumper is shown below.

JPX	Function
JPX1	CAN0 (Between CAN transceiver - 0 CAN connector)
JPX2	CAN0 (Between CPU - CAN transceiver)
JPX3	CAN1 (Between CAN transceiver - CAN connector)
JPX4	CAN1 (Between CPU - CAN transceiver)

Table 4.3.2 (5)

4.3.3 LIN-I/F

(1) LIN-I/F outlline

Two LIN interfaces are mounted as standard.

A block diagram is shown below.

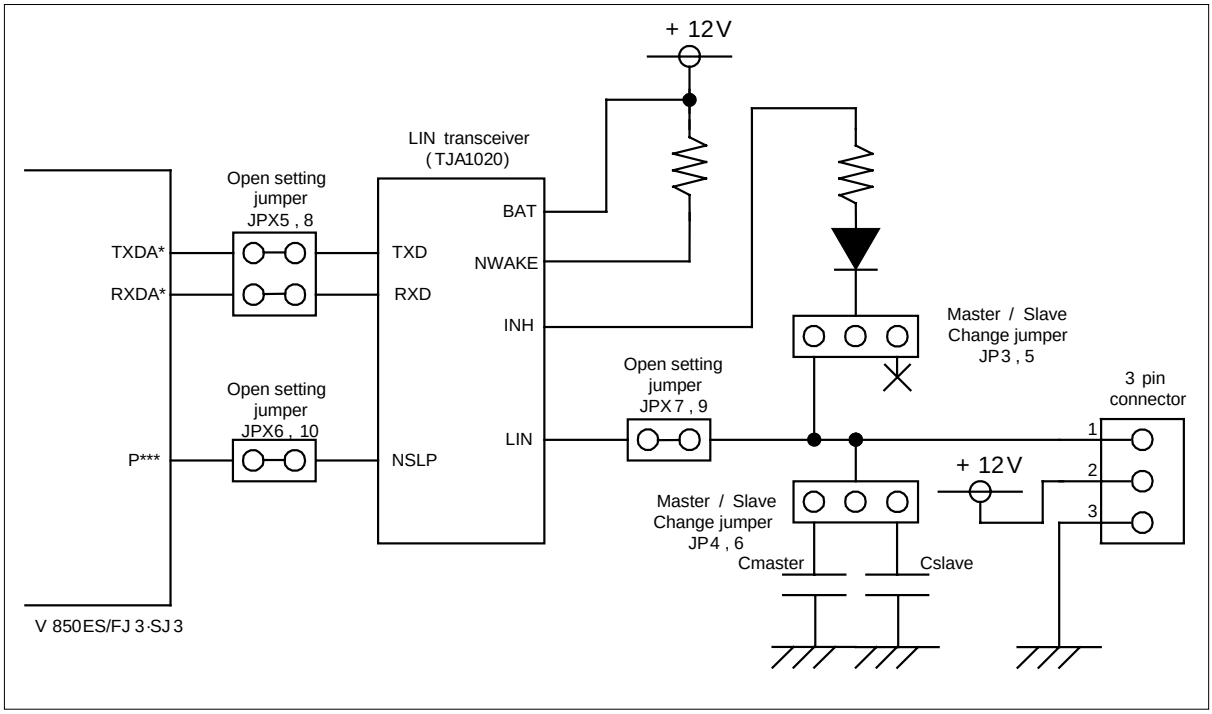


Figure 4.3.3 (1)

(2) LINE-I/F connector (CN3, CN4)

LIN0 is assigned to CN3 and LIN1 is assigned to CN4, respectively.

Connector pin distribution table is shown below.

LIN I/F connector pin description

Pin№	CN3 (LIN0)	CN4 (LIN1)
1	LIN_Bus	LIN_Bus
2	+12V	+12V
3	GND	GND

Table 4.3.3 (2)

Connector part number : IL-SP-S3FP2(J.S.T. Mfg Co.Ltd.)

(3) LIN transceiver

TJA1020T (made by Philips Corp.) are mounted in this board as a LIN transceiver.
Refer to the applicable data sheet for the details of a device.
Connection of CPU and a LIN transceiver is shown below.

LIN0

CPU	TJA1020T	Signal name
RXDD2（P39）	RXD	Reception
P63	NSLP	SLEEP MODE
（pullup）	NWAKE	
TXDD2（P38）	TXD	Transmission
	LIN	LIN
（JP3）	INH	MASTER/SLAVE
	BAT,GND	Powersupply(+12V supply)

Table 4.3.3 (3)-1

LIN1

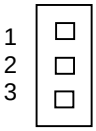
CPU	TJA1020T	Signal name
RXDD3（P80）	RXD	Reception
P64	NSLP	SLEEP MODE
（pullup）	NWAKE	
TXDD3（P81）	TXD	Transmission
	LIN	LIN
（JP5）	INH	MASTER/SLAVE
	BAT,GND	Power supply(+12V supply)

Table 4.3.3 (3)-2

(4) LIN MASTER/SLAVE setting

A jumper is set up by the mode of LIN of operation.

JP3－6



• LIN0 MASTER/SLAVE

Jumper	MASTER setting	SLAVE setting
JP3	2-3 short circuit (default)	1-2 short circuit
JP4	1-2 short circuit (default)	2-3 short circuit

Table 4.3.3 (4)-1

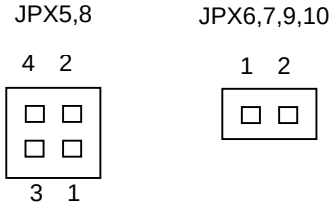
• LIN1 MASTER/SLAVE

Jumper	MASTER setting	SLAVE setting
JP5	2-3 short circuit	1-2 short circuit (default)
JP6	1-2 short circuit	2-3 short circuit (default)

Table 4.3.3 (4)-2

(5) About JPX5-JPX10

Although the pattern connects between 1-2 and between 3-4 of JPX5-JPX8, and between 1-2 of JPX6, JPX9, JPX10, a signal is separable by cutting the pattern on the back side (soldering side) of each jumper. As standard, the following jumper is un-mounting.



The installation part of each jumper is shown below.

JPX	Function
JPX5	LIN0 (Between CPU - LIN transceiver)
JPX6	LIN0 (Between CPU – LIN transceiver NSLP)
JPX7	LIN0 (Between LIN transceiver – LIN connector)
JPX8	LIN1 (Between CPU – LIN transceiver)
JPX9	LIN1 (Between CPU – LIN transceiver NSLP)
JPX10	LIN1 (Between LIN transceiver – LIN connector)

Table 4.3.3 (5)

4.3.4 Expansion connectors (J5, J6)

It is the connector used in case an optional CAN add-in board etc. is connected.
As standard, it is not mounted.

Expansion connectors table

J5			J6		
Pin №	Signal name	Function used on a Board	Pin №	Signal name	Function used on a Board
1	P00	8bit DIP-SW	1	P98/SOB1(A8)	-
2	P10/INTP9	-	2	P912/_SCKB2(A12)	-
3	P01	8bit DIP-SW	3	P99/_SCKB1(A9)	-
4	P11/INTP10	-	4	P913/INTP4(A13)	-
5	P03/INTP0	Push-SW（INTP0）	5	P910/SIB2(A10)	-
6	P32/ASCKA0	8bit DIP-SW	6	P914/INTP5(A14)	-
7	P04/INTP1	-	7	P911/SOB2(A11)	-
8	P35	8bit DIP-SW	8	P915/INTP6(A15)	-
9	P06/INTP3	-	9	PCS0/_CS0	-
10	P41/SOB0	Flash PRO4	10	PCM0/_WAIT	
11	P40/SIB0	Flash PRO4	11	PCS1/_CS1	-
12	P42/_SCKB0	Flash PRO4	12	P36(IETX0)	-
13	P50/KR0	8bit DIP-SW	13	PCS2/_CS2	-
14	P53/KR3/DDO	N-Wire	14	P37(IERX0)	-
15	P51/KR1	8bit DIP-SW	15	PCS3/_CS3	-
16	P54/KR4/DCK	N-Wire	16	PCT5	8bit DIP-SW
17	P52/KR2/DDI	N-Wire	17	P73/ANI3	-
18	P55/KR5/DMS	N-Wire	18	PCT7	8bit DIP-SW
19	P90/TXDA1(A0)	-	19	P72/ANI2	-
20	P95(A5)	-	20	P60/INTP11	Expansion CAN（CAN2）RS
21	P91/RXDA1(A1)	-	21	P61/INTP12	Expansion CAN（CAN3）RS
22	P96(A6)	-	22	P70/ANI0	
23	P92(A2)	-	23	P71/ANI1	-
24	P97/SIB1(A7)	-	24	P65/CTXD2	Expansion CAN（CAN2）TXD
25	P93(A3)	-	25	P66/CRXD2	Expansion CAN（CAN2）RXD
26	CPOW		26	**+5V**	
27	P94(A4)	-	27	P67/CTXD3	Expansion CAN（CAN3）TXD
28	_RESET	Push-SW（RESET）	28	P68/CRXD3	Expansion CAN（CAN3）RXD
29	**GND**		29	+12V	-
30	**GND**		30	**GND**	

Table 4.3.4

The pull-up of each signal is carried out by resistance 47kΩ.
CPOW=CPU power supply　FJ3:+5V,　SJ3:+3.3V

4.3.5 7-segment LED (LED1)

The seven-segment LED is mounted on a board.

The LED can be statically switched on the light or put out from the port of CPU.

In case you make each segment turn on, please set a corresponding port as "0."

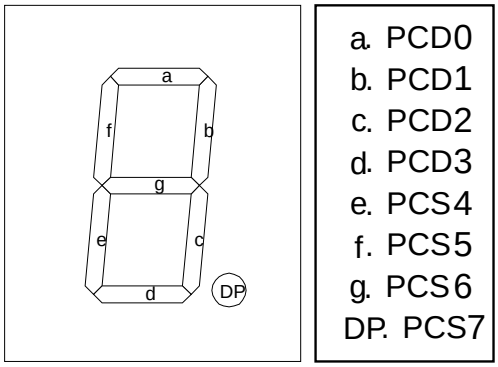


Figure 4.3.5

Segment	Correspondence port	Light/Extinguish	default
a	PCD0	0 / 1	1 (pullup)
b	PCD1	0 / 1	1 (pullup)
c	PCD2	0 / 1	1 (pullup)
d	PCD3	0 / 1	1 (pullup)
e	PCS4	0 / 1	1 (pullup)
f	PCS5	0 / 1	1 (pullup)
g	PCS6	0 / 1	1 (pullup)
D.P.	PCS7	0 / 1	1 (pullup)

Table 4.3.5

4.3.6 8-bit DIP SW (SW1)

8-bit DIP SW is mounted on a board.

ON/OFF of DIP SW can be checked in a CPU port.

If DIP SW is turned "ON", a port will be set to "0", and a port will be set to "1" if it turns "OFF."

bit	Port
DIP-SW1	P50
DIP-SW2	P51
DIP-SW3	PCT5
DIP-SW4	PCT7
DIP-SW5	P32
DIP-SW6	P35
DIP-SW7	P00
DIP-SW8	P01

Table 4.3.6

4.3.7 RESET

(1) RESET overview

When the time of power on or SW4 are pushed, reset starts a board.

It is a RESET signal at the MINICUBE or FL-PR4 use and MINICUBE2 use time, and composition differs.

A reset signal block diagram is shown below.

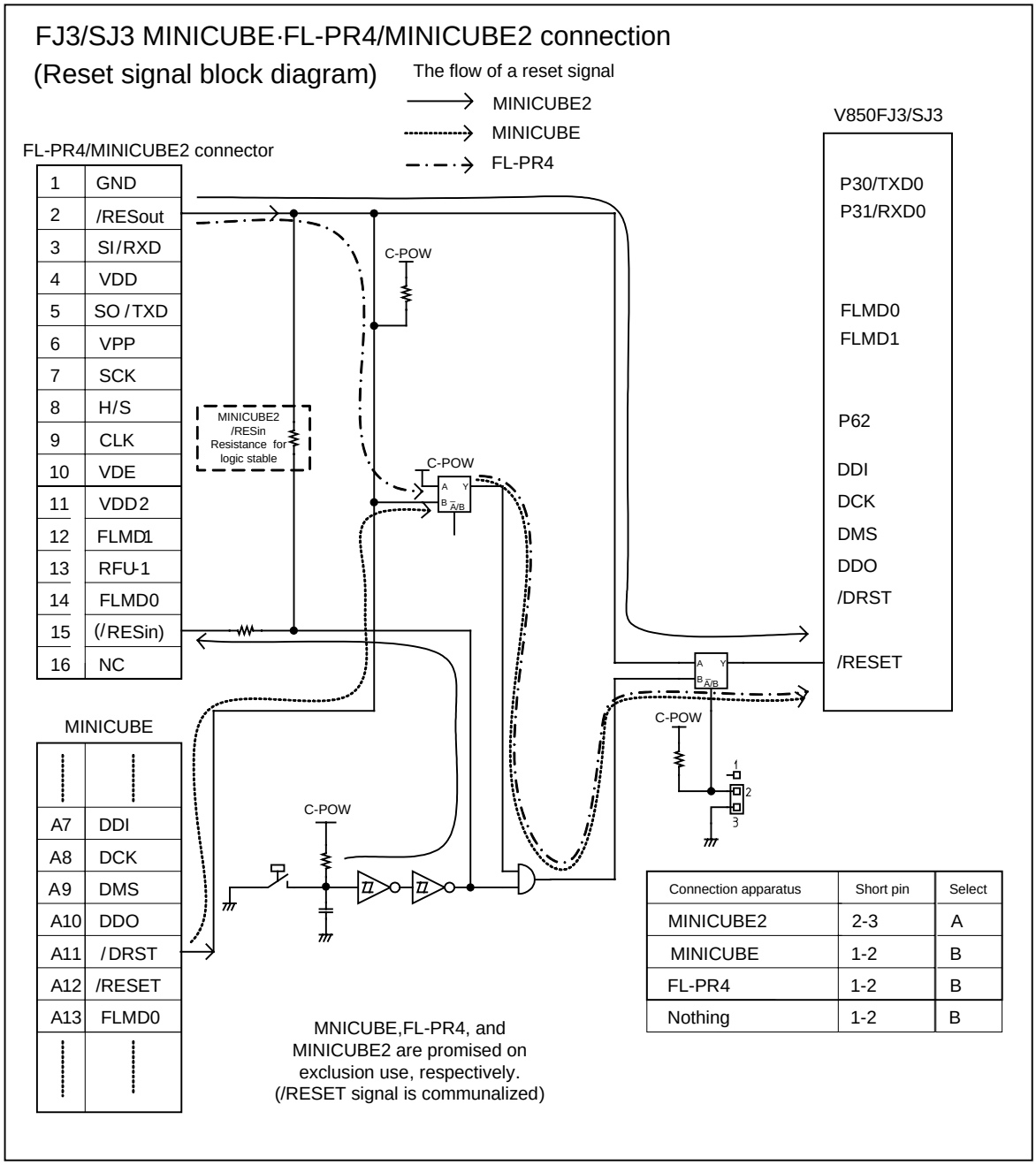
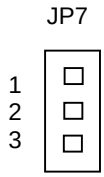


Figure 4.3.7

(2)RESET signal setting (JP7)

A setup of a RESET signal changes with apparatus connected.

JP7 performs a setup.



JP7	Function
1-2 short circuit	Normal use, During connecting FL-PR4, During connecting MINICUBE (default)
2-3 short circuit	During connecting MINICUBE2

Table 4.3.7 (2)

In case FL-PR4 or MINICUBE are used, a JP7 short pin is set to the "1-2" side, and it is set as the course of dashed-and-dotted line (FL-PR4) and a dotted line (MINICUBE).

(Refer to Figure 4.3.7)

In case MINICUBE2 is used, a JP7 short pin is set to the "2-3" side, and it is set as the course of a solid line (MINICUBE2).

Please use a JP7 short pin for the "1-2" side at the time of real operation, setting it up (when you do not use a debugger).

(3)RESET SW (SW4)

If SW4 is pushed, CPU and an evaluation board will be in a reset state.

4.3.8 INTP0 SW (SW2)

SW2 on a board is connected to P03-/INTP0 port.

A push on SW2 inputs "0" into P03-/INTP0 port.

4.3.9 NMI SW (SW3)

SW3 on a board is connected to P02-/NMI port.

A push on SW3 inputs "0" into P02-NMI port.

4.3.10 CLOCK

(1) Main Clock

The crystal oscillator is connected to X1 and X2 terminals of CPU.
Oscillation frequency is 6MHz in FJ3, and it is 4MHz in SJ3.
Since the socket is mounted, a crystal oscillator is exchangeable if needed. Please purchase a HC49 U/S type crystal oscillator.
Since it operates by the CPU internal clock by the default, in case an external clock is used, an inside register setup of CPU is changed.
Please refer to an applicable CPU user's manual for details.

(2)Sub Clock

The crystal oscillator is connected to XT1 and XT2 terminals of CPU. Oscillation frequency is 32.768kHz.
Since it is soldered directly, crystal is unexchangeable.

4.3.11 USB

(1) USB overview

USB connection is made using the UART interface of CPU.

USB-UART interface device FT232R is mounted and USB is changed into UART.

The USB section block diagram is shown below.

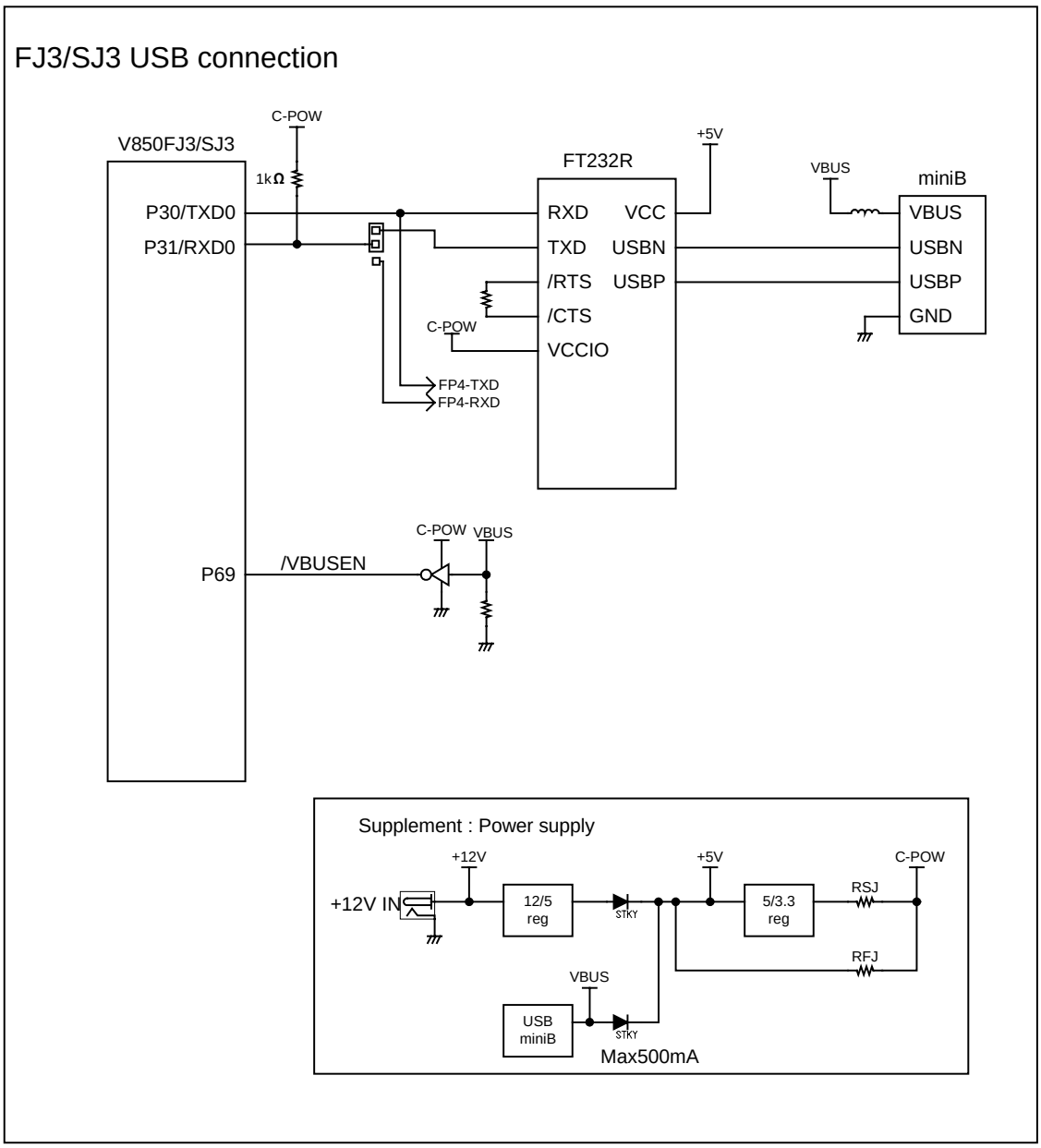
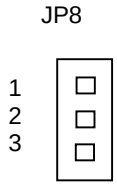


Figure 4.3.11

(2) USB setting

With a flash write-in circuit, since P31 (RXD0) is common, please set a jumper (JP8) to the "1-2" side, and perform USB communication.



JP8	CPU RXD0（P31）
1-2 short circuit	TXD of USB connects. (default)
2-3 short circuit	TXD of CN5 connects.

Table 4.3.11 (2)

(3) The check of USB cable insertion and extraction

The insertion and extraction state of a USB cable can be checked by checking the level of P69.

P69 input	state
Lo	USB cable connecting
Hi	USB cable un-connecting

Table 4.3.11 (3)

Refer to the user's manual etc. for a setup of P69.

(4) About driver software

It is downloadable from the homepage of Future Technology Devices International Corp.

(5) USB bus power

VBUS which is the bus power of USB is set “DIODE OR” to +5V power supply of this board.
When making it operate with this board simple substance, it can operate only by connecting USB with PC.
However, since drive current is restricted to 500mA as a standard of VBUS which is bus power, the drive of CAN is not recommended.
(Please confirm that the whole board consumption current is 500mA or less)
Since +12V are required about LIN, it cannot operate by USB bus power.
When you operate LIN, please supply +12V from this board power supply jack.

4.3.12 Evaluation environment

(1) Overview

The development environment which can be used on this board is as follows.

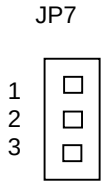
Built-in FLASH writing	-	FL-PR4
Debugging	-	MINICUBE, MINICUBE2

It is designing on the assumption that the three above-mentioned kinds.

This board mounts the connector for FL-PR4 connection in built-in FLASH writing.
The connector for FL-PR4 connection is as common as MINICUBE2.
Moreover, the connector for MINICUBE connection is mounted.
A block diagram is shown in the following clause.
In circuit composition, FL-PR4, and MINICUBE2 and MINICUBE constitute exclusion use as a premise.
If FL-PR4 or MINICUBE2, and MINICUBE are simultaneously connected to a connector, since a signal collision will occur, please avoid simultaneous use absolutely.

(2) Setup

A setup of the following jumper (JP7) is changed according to the development environment to be used.



JP7	Function
	Normal use, During connecting FL-PR4, During connecting MINICUBE (default)
2-3 short circuit	During connecting MINICUBE2

Table 4.3.12 (2)

In case FL-PR4 and MINICUBE are used, a JP7 short pin is set to the "1-2" side, and it is set as the course of dashed-and-dotted line (FL-PR4) and a dotted line (MINICUBE).
(Refer to Figure 4.3.7)
In case MINICUBE2 is used, a JP7 short pin is set to the "2-3" side, and it is set as the course of solid line (MINICUBE2).
Please use a JP7 short pin for the "1-2" side at the time of real operation, setting it up (when you do not use a debugger).

MINICUBE and FL-PR4, MINICUBE2 connection block diagram

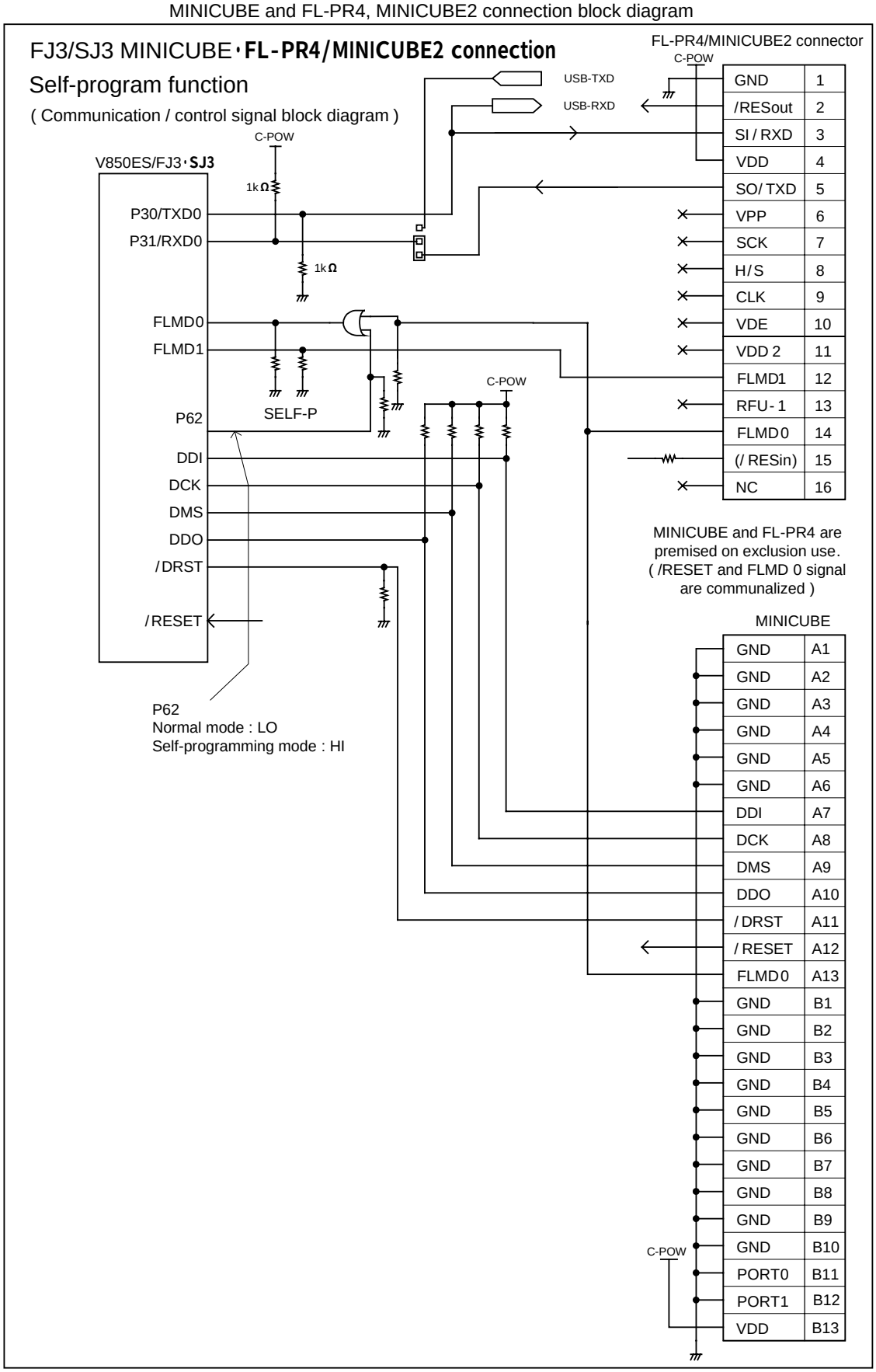


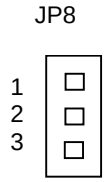
Figure 4.3.12

(3) About communication with CPU

FL-PR4 and MINICUBE2 support only communication by UART for circuit simplification.

* "3-wire serial" mode is not supported.Please use FL-PR4 and MINICUBE2 by "UART" mode.
(Please refer to the user's manual of each equipment for details)

With a later USB circuit, since P31 (RXD0) is common, please set a jumper (JP8) to the "2-3" side, and perform debugging and flash writing.



JP8	CPU RXD0 (P31)
1-2 short circuit	TXD of USB connects (default)
2-3 short circuit	TXD of CN5 connects

Table 4.3.12 (3)

(4)Self-programming

By operating FLMD0 signal by P62, a self-program function is realizable.

P62 is connected to FLMD0 through an OR gate.

P62 will become effective if FLMD0 from a debugger and a flash writer is made into a "LO" level, or in the state of un-connecting a debugger and a flash writer.

P62 output	Status	Explanation / Conditions
Lo	Normal	Normal state
Hi	Self-programming MODE	FLMD0 of a debugger and a flash writer "Lo" or it un-connects

Table 4.3.12 (4)

Refer to the user's manual etc. for a setup of P62.

Refer to the user's manual for the details of self programming.

4.3.13 The connector for MINICUBE (CN6)

It is a connector for connecting MINICUBE which is a target CPU debugger.

No.	Signal	No.	Signal
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	DDI	B7	GND
A8	DCK	B8	GND
A9	DMS	B9	GND
A10	DDO	B10	GND
A11	/DRST	B11	PORT0
A12	/RESET	B12	PORT1
A13	FLMD0	B13	VDD

Table 4.3.13

4.3.14 The connector for FL-PR4, MINICUBE2 (CN5)

It is a connector for connecting MINICUBE2 which is a target CPU debugger.
Moreover, it is as common as the connection connector of FL-PR4 which is a FLASH write-in tool with a built-in CPU.

PinNo.	Signal	V850ES/FJ3
1	GND	GND
2	_RESET	_RESET
3	SI/RxD	P40/SIB0 or P31/RXDD0
4	VDD	EVDD
5	SO/TxD	P41/SOB0 or P30/TXDD0
6	VPP	N.C.
7	SCK	P42/SCKB0
8	H/S	PCM0
9	CLK	N.C.
10	VDE	N.C.
11	VDD2	N.C.
12	FLMD1	N.C.
13	RFU-1	N.C.
14	FLMD0	FLMD0
15	/RESETin	N.C.
16	N.C.	N.C.

Table 4.3.14

The "/RESETin" of a No. 15 pin is the reset signal passed to MINICUBE2. It is not used at the time of FL-PR4 connection.

4.3.15 The connector for CPU I/O pins check

The through hole for checking each terminal of CPU is arranged around a CPU chip.
The column from which the CPU pin number is "-" is not pulled out to the connector for a check.
(Each signal name has indicated the thing of FJ3)

(1) J1

No	Signal name	CPUpin	No	Signal name	CPUpin
1	(GND)	-	2	(GND)	-
3	P10/INT9	3	4	P11/INT10	4
5	(GND)	-	6	P00/…	6
7	P01/…	7	8	FLMD0	8
9	(GND)	-	10	(GND)	-
11	(GND)	-	12	(GND)	-
13	(GND)	-	14	/RESET	14
15	(GND)	-	16	(GND)	-
17	P02/NMI	17	18	P03/INT0	18
19	P04/INT1/…	19	20	P05/INT2	20
21	P06/INT3/…	21	22	P40/…	22
23	P41/…	23	24	P42/…	24
25	P30/TXD0	25	26	P31/RXD0/…	26
27	P32/…	27	28	P33/…	28
29	P34/…	29	30	P35/…	30
31	P36/CTXD1	31	32	P37/CRTX1	32
33	(GND)	-	34	(GND)	-
35	P38/TXD2	35	36	P39/RXD2/…	36

Table 4.3.15 (1)

(2) J2

No	Signal name	CPUpin	No	Signal name	CPUpin
1	P50/KR0/…	37	2	P51/KR1/…	38
3	P52/KR2/…	39	4	P53/KR3/…	40
5	P54/KR4/…	41	6	P55/KR5/…	42
7	P60/INT11	43	8	P61/INT12	44
9	P62/INT12/…	45	10	P63/SCKB3	46
11	P64/SCKB3	47	12	P65/CTXD2	48
13	P66/CRXD2	49	14	P67/CTXD3	50
15	P68/CRXD3	51	16	P69	52
17	P610/…	53	18	P611/…	54
19	P612/…	55	20	P613/…	56
21	P614	57	22	P615	58
23	P80/RXD3/…	59	24	P81/TXD3	60
25	P90/KR6/…	61	26	P91/KR7/…	62
27	P92/…	63	28	P93/…	64
29	P94/…	65	30	P95/…	66
31	P96/…	67	32	P97/SIB1/…	68
33	P98/SOB1/…	69	34	P99/SCKB1/..	70
35	P910/SIB2/…	71	36	P911/SOB2/…	72

Table 4.3.15 (2)

(3) J3

No	Signal name	CPUpin	No	Signal name	CPUpin
1	P912/SCKB2/…	73	2	P913/INT4/…	74
3	P914/INT5/…	75	4	P915/INT6/…	76
5	PCD0	77	6	PCD1	78
7	PCD2	79	8	PCD3	80
9	PCS0/CS0	81	10	PCS1/CS1	82
11	PCS2/CS2	83	12	PCS3/CS3	84
13	PCM0/WAIT	85	14	PCM1/CLKO	86
15	PCM2/HLDAK	87	16	PCM3/HLDRQ	88
17	PCM4	89	18	PCM5	90
19	PCS4	91	20	PCS5	92
21	PCS6	93	22	PCS7	96
23	PCT0/WR0	95	24	PCT1/WR1	94
25	PCT2	97	26	PCT3	98
27	PCT4/RD	99	28	PCT5	100
29	PCT6/ASTB	101	30	PCT7	102
31	(GND)	103	32	(GND)	104
33	PDL0/AD0	105	34	PDL1/AD1	106
35	PDL2/AD2	107	36	PDL3/AD3	108

Table 4.3.15 (3)

(4) J4

No	Signal name	CPUpin	No	Signal name	CPUpin
1	PDL4/AD4	109	2	PDL5/FLMD1/…	110
3	PDL6/AD6	111	4	PDL7/AD7	112
5	PDL8/AD8	113	6	PDL9/AD9	114
7	PDL10/AD10	115	8	PDL11/AD11	116
9	PDL12/AD12	117	10	PDL13/AD13	118
11	PDL14/AD14	119	12	PDL15/AD15	120
13	P127/ANI23	121	14	P126/ANI22	122
15	P125/ANI21	123	16	P124/ANI20	124
17	P123/ANI19	125	18	P122/ANI18	126
19	P121/ANI17	127	20	P120/ANI16	128
21	P715/ANI15	129	22	P714/ANI14	130
23	P713/ANI13	131	24	P712/ANI12	132
25	P711/ANI11	133	26	P713/ANI10	134
27	P79/ANI9	135	28	P78/ANI8	136
29	P77/ANI7	137	30	P76/ANI6	138
31	P75/ANI5	139	32	P74/ANI4	140
33	P73/ANI3	141	34	P72/ANI2	142
35	P71/ANI1	143	36	P70/ANI0	144

Table 4.3.15 (4)

4.4 Memory map

(1) V850ES/FJ3 'F3380

Built-in FLASH 512KB, Built-in RAM32KB

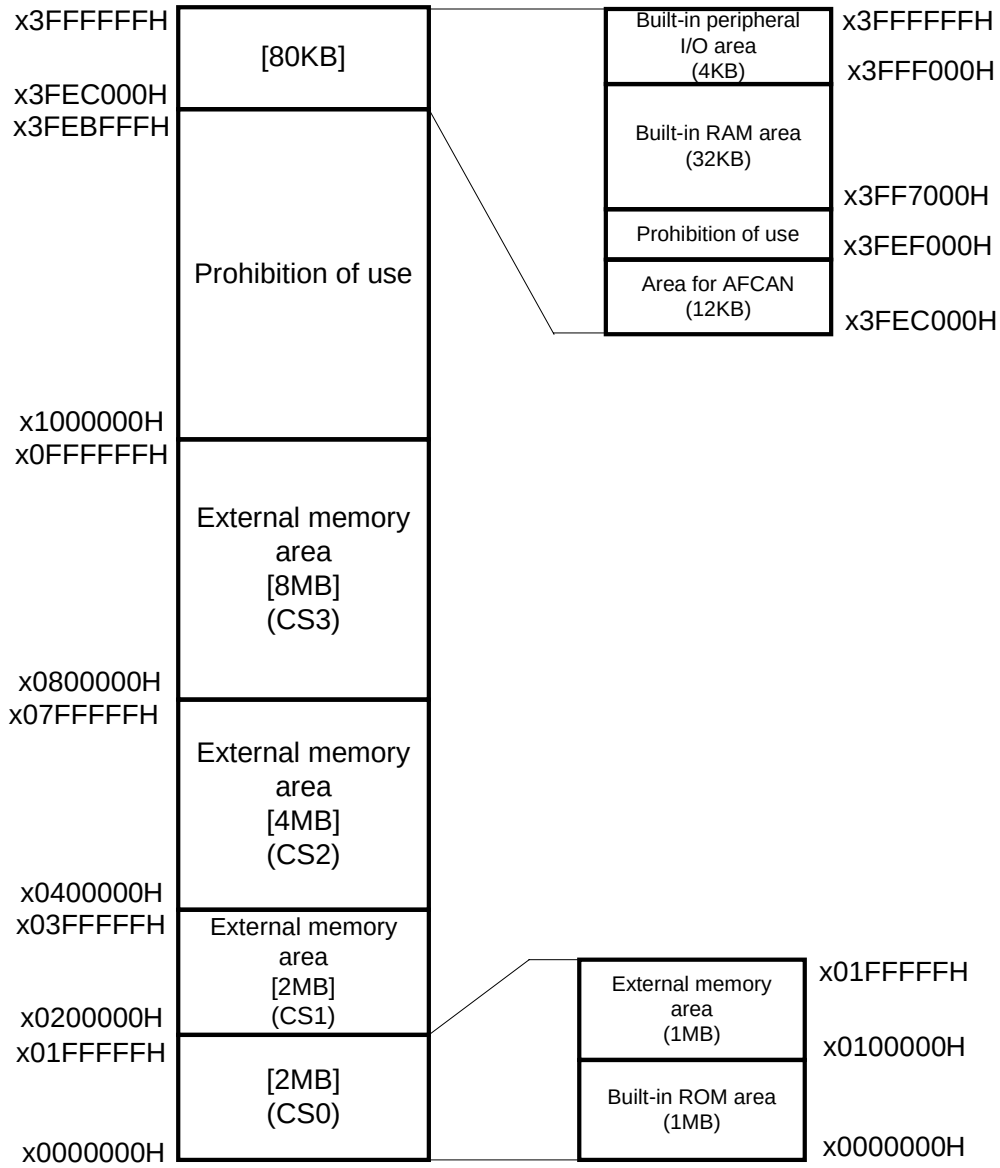


Figure 4.4 (1)

(2) V850ES/SJ3 'F3368

Built-in FLASH 1024kB, Built-in RAM60kB

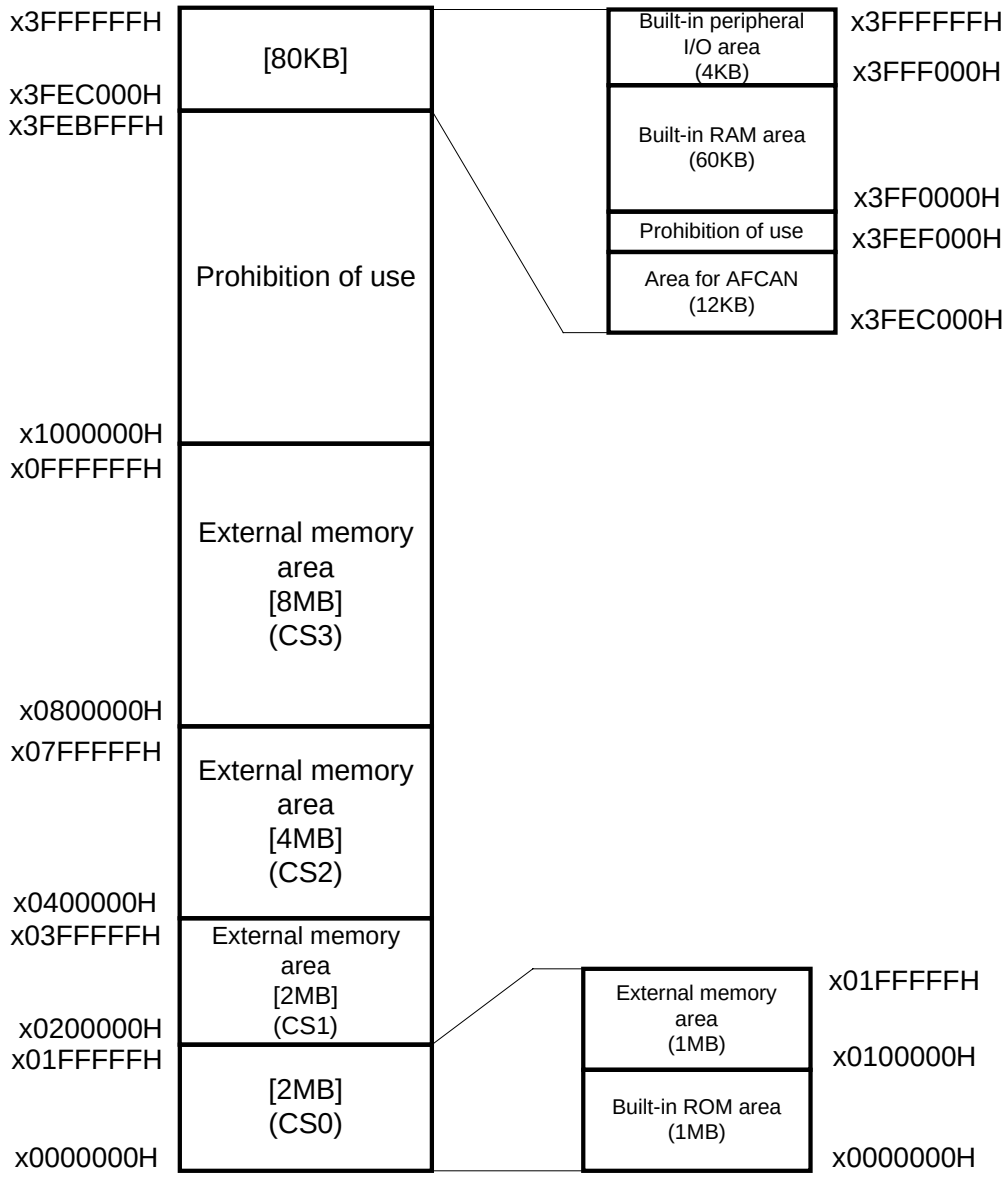


Figure 4.4 (2)

4.5 Notes at the time of user circuitry

In adding and connecting a user circuit at an evaluation board, please consider the following notes to the design and manufacture which cannot receive influence of a noise etc. in reference easily.
Moreover, there are restrictions matters, such as drive current, in each terminal. Please refer to these notes and a correspondence CPU user's manual, and use it within rating.

4.5.1 Consumption current

The total combined consumption current of this board and expansion boards must be 0.3 A or less, due to connector performance factors.
When the current exceeding 0.3A is required, a heat sink is needed for U13.
Please attach the optimal heat sink after having a heat design carried out , or contact to our company in that case.
If the current more than 0.3A is passed without a heat sink, U13 generates heat and there is danger, such as a burn and a fire.
Moreover, power supply supply stops by the shutdown function which U13 has.
The supplied AC adapter is rated for 12 V, 0.5 A or higher, but the rating may differ depending on the shipment lot.

4.5.2 I/O signals

Each signal line currently outputted to J3 and J4 is outputted to the connector, after pulling up by 47kΩ.
Pay attention to pattern damage, pattern bridge, etc., and implement measures as needed, such as removing mounted parts.
For the specifications of each pin and the electrical specifications, refer to the correspondence CPU user's manual.

4.6 A jumper setup at the time of shipment

A setup of the jumper at the time of shipment is as in the following tables.

No	State	Function
JP1	1-2 OPEN	CAN0 no terminator
	3-4 OPEN	
JP2	1-2 OPEN	CAN1no terminator
	3-4 OPEN	
JP3	2-3 SHORT	LIN0 master
JP4	1-2 SHORT	LIN0 master
JP5	2-3 SHORT	LIN1 master
JP6	1-2 SHORT	LIN1 master
JP7	1-2 SHORT	Reset normal use
JP8	1-2 SHORT	RXD0,USB(UART) use

Table 4.6

5. CAN expansion board

This product is a board for CAN interface expansion developed for the CEB-V850ES/FJ2.
(As standard, it is not attached.)

5.1 Specifications

The CAN expansion board, which expands the number of CAN channels by 2 channels, is used connected to the J5 and J6 connectors of the CEB-V850ES/FJ3.

5.2 Block diagram

CAN expansion board block diagram

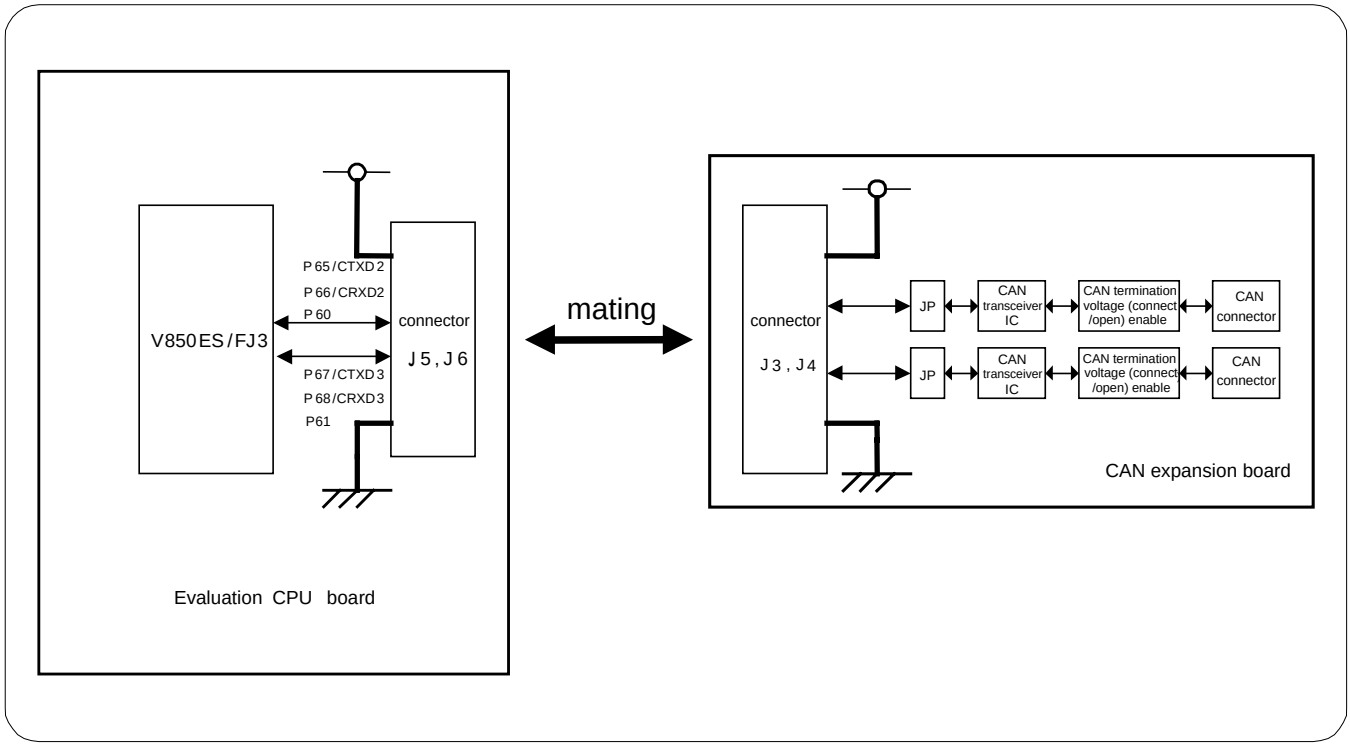


Figure 5.2

5.3 Board size

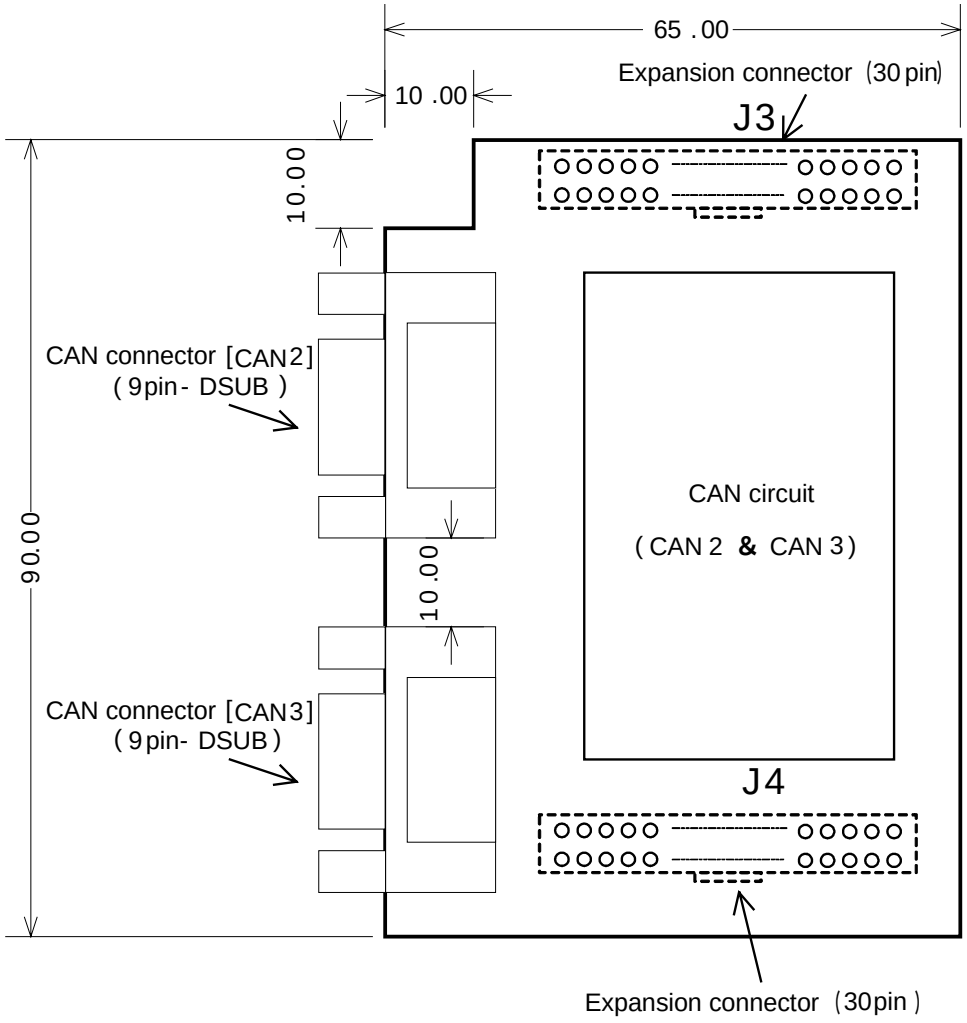


Figure 5.3

5.4 External connectors

Table of Connection connectors (J3, J4)

J3			J4		
Pin No.	Signal Name	Usage Type with CAN Expansion Board	Pin No.	Signal Name	Usage Type with CAN Expansion Board
1	P00	N.C	1	P98/SOB1(A8)	N.C
2	P10/INTP9	N.C	2	P912/_SCKB2(A12)	N.C
3	P01	N.C	3	P99/_SCKB1(A9)	N.C
4	P11/INTP10	N.C	4	P913/INTP4(A13)	N.C
5	P03/INTP0	N.C	5	P910/SIB2(A10)	N.C
6	P32/ASCKA0	N.C	6	P914/INTP5(A14)	N.C
7	P04/INTP1	N.C	7	P911/SOB2(A11)	N.C
8	P35	N.C	8	P915/INTP6(A15)	N.C
9	P06/INTP3	N.C	9	PCS0/_CS0	N.C
10	P41/SOB0	N.C	10	PCM0/_WAIT	N.C
11	P40/SIB0	N.C	11	PCS1/_CS1	N.C
12	P42/_SCKB0	N.C	12	P36(IETX0)	N.C
13	P50/KR0	N.C	13	PCS2/_CS2	N.C
14	P53/KR3/DDO	N.C	14	P37(IERX0)	N.C
15	P51/KR1	N.C	15	PCS3/_CS3	N.C
16	P54/KR4/DCK	N.C	16	PCT5	N.C
17	P52/KR2/DDI	N.C	17	P73/ANI3	N.C
18	P55/KR5/DMS	N.C	18	PCT7	N.C
19	P90/TXDA1(A0)	N.C	19	P72/ANI2	N.C
20	P95(A5)	N.C	20	P60/INTP11	Expansion CAN(CAN2)RS
21	P91/RXDA1(A1)	N.C	21	P61/INTP12	Expansion CAN(CAN3)RS
22	P96(A6)	N.C	22	P70/ANI0	N.C
23	P92(A2)	N.C	23	P71/ANI1	N.C
24	P97/SIB1(A7)	N.C	24	P65/CTXD2	Expansion CAN(CAN2)TXD
25	P93(A3)	N.C	25	P66/CRXD2	Expansion CAN(CAN2)RXD
26	CPOW	N.C	26	**+5V**	**+5V**
27	P94(A4)	N.C	27	P67/CTXD3	Expansion CAN(CAN3)TXD
28	_RESET	N.C	28	P68/CRXD3	Expansion CAN(CAN3)RXD
29	**GND**	N.C	29	+12V	N.C
30	**GND**	**GND**	30	**GND**	**GND**

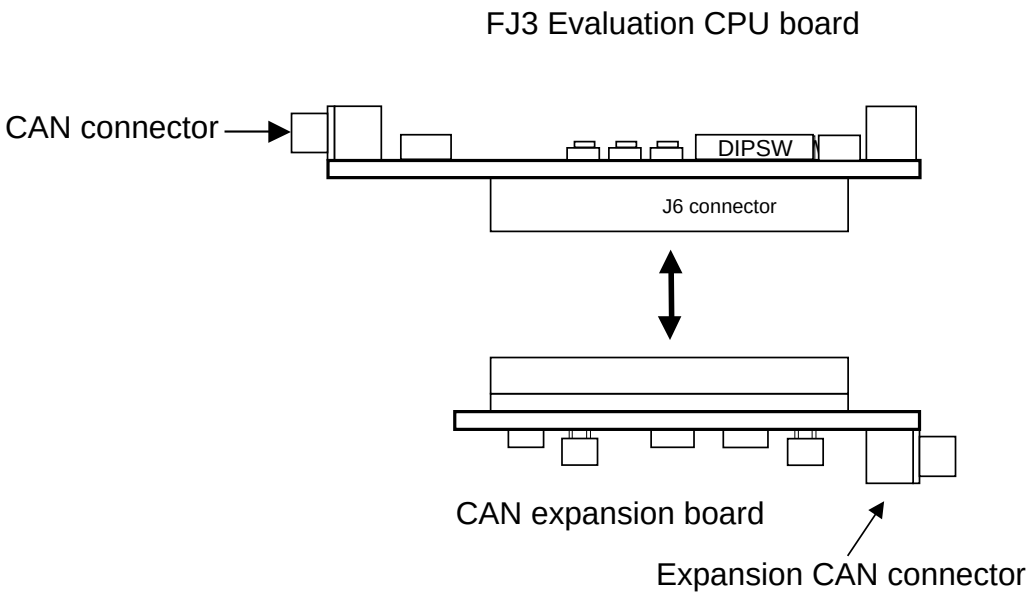
Table 5.4

* J3 is connected to J5 of CEB-V850ES/FJ3.
* J4 is connected to J6 of CEB-V850ES/FJ3.

5.5 Evaluation board mating

The following figure illustrates mating of the V850ES/FJ3 evaluation CPU board and expansion board.

《Longitudinal View》



《Transversal View》

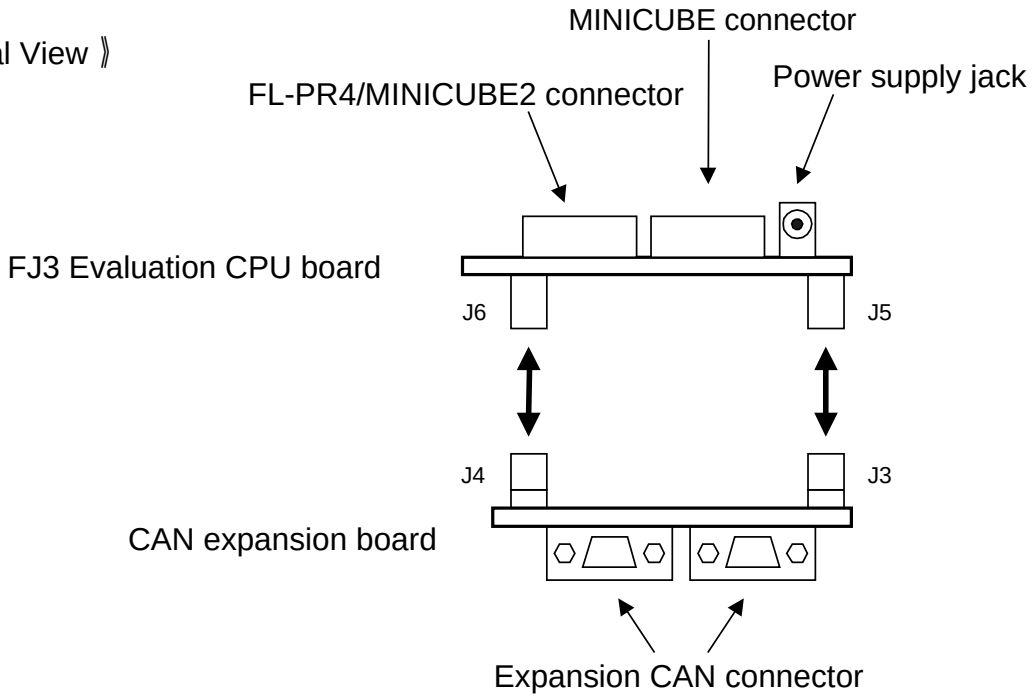


Figure 5.1.5

Revision History

Edition	Description	Page(s)
The 1.0 th Apr. 2007	The first-edition issue	