TK-850/SG2+UZ
Hardware User's Manual

TESSERA TECHNOLOGY INC.

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1 TK-850/SG2+UZ

V850ES/SG2 is the NEC Electronics 32bit single chip microcomputer.
The features and hardware specification of an evaluation board (TK-850/SG2+UZ CPU board) of V850ES/SG2 with UZ2400 RF board (Uniband Electronic Corporation) are described.

1.1 Features

Features of the TK-850/SG2+UZ CPU board are as follows.

●The evaluation board used the NEC Electronics 32bit single chip microcontroller. (μPD70F3281YGC).
All of the ROM, RAM and circumference circuit are efficiently built in one chip on a single board.
●High-speed operation is realized via the 20MHz internal clock.
●32.768KHz sub-clock standard equipment
●The high speed RAM: 32K-byte and the flash memory 384 K-byte are built into CPU chip.
●TK-850/SG2+UZ contain UZ2400 RF board (2.4GHz、Accordance with IEEE802.15.4) made by Uniband Electronic Corporation.(http://www.ubec.com.tw/index.html)※
Affixed antenna : Made by Gigaant, Titanis （http://www.gigaant.com/）※
●17 I/O ports are equipped for expand use.
●TK-850/SG2+UZ contain a temperature sensor.(Made by SII, S-8120C http://www.sii.co.jp/)
●The board itself is quite and easy to handle; CPU board size: 91mm×62mm, The size of include RF transceiver: 103mm×62mm

※ Please inquire direct to the parts maker about specification of UZ2400 RF board, antenna and temperature sensor.

1.2 Hardware specification

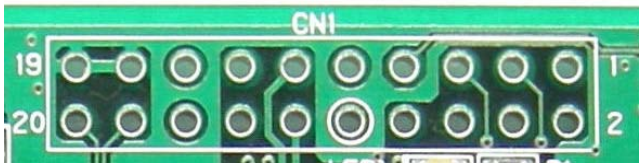
Item		Details
CPU	Parts number	μPD70F3281YGC-8EU
	Operation with main clock	20MHz
	Clock	Main ：5MHz、Sub：32.768KHz
	Internal flash memory	384KB
	Internal RAM	32KB
	Operation voltage	3.3V
	I/O voltage	3.3V
	Special mention	IIC included、CAN included
USB interface		Mini USB 1 channel
Serial interface		Equipped with Synchronous/Asynchronous header pin.
Ethernet inter face		RJ-45(10/100M) 1Port MAC address setup：External EEPROM State indication LED：2
CAN		T/H pattern for external connection
RF board		UZ2400 RF Board
Temperature sensor		Temperature sensor x 1
LED		Red x 4, LED 1 – 4: Multipurpose Green x 3, LED 5: Power, LED 6: LAN, LED 7: LINK
Multipurpose input		4bit Slide switch x 1, Push switch x 2
Reset Switch		Push switch x 1
N-WIRE/MiniCube interface		Not mount （Tokyo eleteck Corp :SICA2P20S）
On board Flash memory writing		Possible
Power supply		5.0V(USB supply)、6.0V(battery supply)

1.3 Terminal list

It is a terminal table of CN1, CN3 and CN4 of CPU board.

CN1 terminal list (HONDA CONNECTORS FFC-20BMEP1:Not mount)

CN1	Signal name	Terminal CPU name at connection destination	Notes
1	VDD	VDD	
2	P36	P36/CTXD0/IETX0	
3	P37	P37/CRXD0/IERX0	
4	P38	P38/TXDA2/SDA00	
5	P39	P39/RXDA2/SCL00	
6	P53	P53/SIB2/KR3/TIQ00/TOQ00/RTP03/DDO	Both use with N-Wire
7	P54	P54/SOB2/KR4/RTP04/DCK	Both use with N-Wire
8	P55	P55/SCKB2/KR5/RTP05/DMS	Both use with N-Wire
9	P70	P70/ANI0	
10	P71	P71/ANI1	
11	P72	P72/ANI2	
12	P73	P73/ANI3	
13	PCM1	PCM1/CLKOUT	
14	PCM2	PCM2/HLDAK	
15	PCM3	PCM3/HLDRQ	
16	PCT1	PCT1/WR1	
17	GND	GND	
18	PDH4	PDH4/A20	
19	GND	GND	
20	PDH5	PDH5/A21	



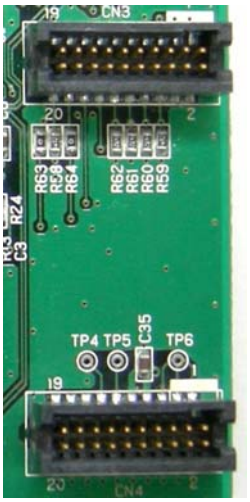
CN1Pin configuration

CN3 terminal list (SAMTEC TFM-110-02-S-D-A-K-TR)

CN3	Signal name	Terminal CPU name at connection destination	Notes
1	GND	GND	
2			N.C.
3	VREG_EN	P02/NMI	Output from CPU
4			N.C.
5	RESn	P03/INTP0/ADTRG	Output from CPU
6	FIFO	P10/ANO0	Input to CPU
7			N.C.
8	FIFOP	P06/INTP3	Input to CPU
9			N.C.
10	CCA	P11/ANO1	Input to CPU
11			N.C.
12	SFD	P33/TIP01/TOP01	Input to CPU
13			N.C.
14	CSn	P34/TIP10/TOP10	Output from CPU
15			N.C.
16	SCLK	P42/SCKB0	Output from CPU
17			N.C.
18	SI	P41/SOB0	Output from CPU
19	GND	GND	
20	SO	P40/SIB0	Input to CPU

CN4 terminal list (SAMTEC TFM-110-02-S-D-A-K-TR)

CN4	Signal name	Terminal CPU name at connection destination	Notes
1	TP6		
2	GND	GND	
3	TP6		
4	GND	GND	
5	TP6		
6	GND	GND	
7	3.3V		
8	GND	GND	
9	3.3V		
10	GND	GND	
11	TP5		
12	GND	GND	
13	TP4		
14	GND	GND	
15			N.C.
16	GND	GND	
17			N.C.
18	GND	GND	
19			N.C.
20	GND	GND	



CN3,CN4 Pin Configuration

2 Switches and LED

2.1 SW1、JP1

Bit1～4 of SW 1is dip switch for operation mode setting, bit5～8 are connected to P74～P77 for multipurpose input .

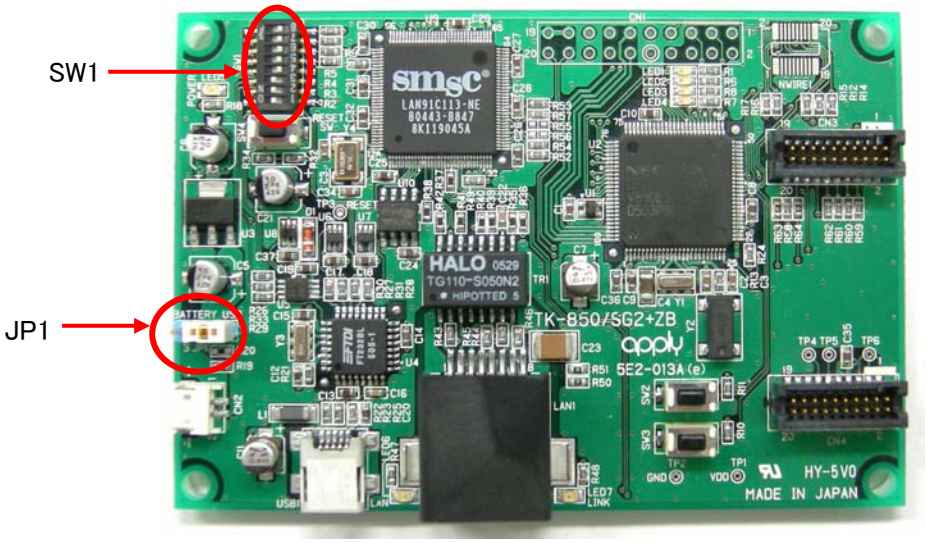
JP1 is a jumper to select a power source.

2.1.1 Flash Programming Mode

Flash EEPROM on the CPU can be programmed using the attached software “PG-FPL” in your PC, if the following switch and jumper setting is made.

Flash programming mode setting

SW1	Bit 1	ON
	Bit 2	OFF
	Bit 3	ON
	Bit 4	ON
JP1		USB side (1-2pin short)



2.1.2 ID850-TK Mode

The following setting activates the On-chip debug functions on the CPU.

ID850-TK Mode setting

SW1	Bit 1	ON
	Bit 2	ON
	Bit 3	ON
	Bit 4	OFF
JP1		USB side (1-2pin short)

※1 **ID850-TK is using P30/TXDA0,P31/RXDA0 pin to make communication to the host machine. Therefore those pin can not use on On-chip debag mode.**

2.1.3 N-Wire Connecting Mode

Please change to the following settings when you connect to N-Wire emulator.

N-Wire Connecting Mode setting

SW1	Bit 1	ON or OFF ※2
	Bit 2	OFF
	Bit 3	OFF
	Bit 4	OFF
JP1		USB Side (1-2pin short)

※2 please set ON, if you make COM communication to host machine using the **P30/TXDA0,P31/RXDA0** pin.

2.1.4 Normal Operation Mode

Please change to the following settings when you execute the program normally.

Normal Operation Mode

SW1	Bit 1	OFF
	Bit 2	OFF
	Bit 3	OFF
	Bit 4	OFF
JP1		See below

Please select the JP1 by power source.

JP1Setting

USB Power	USB (1-2pin short)
Battery	CN2 (2-3pin short)

2.1.5 General purpose setting port

Bit5-8 of SW1 is general purpose setting port.

It becomes “Low” because it connected to GND. if the switch is ON , and it becomes “High” because it connected to 10kΩ pull-up resister . if the switch is OFF.

SW 1terminal list

SW1	Signal name	Terminal CPU name at connection destination	Notes
Bit 5	P74	P74/ANI4	
Bit 6	P75	P75/ANI5	
Bit 7	P76	P76/ANI6	
Bit 8	P77	P77/ANI7	

2.2 SW2, SW3

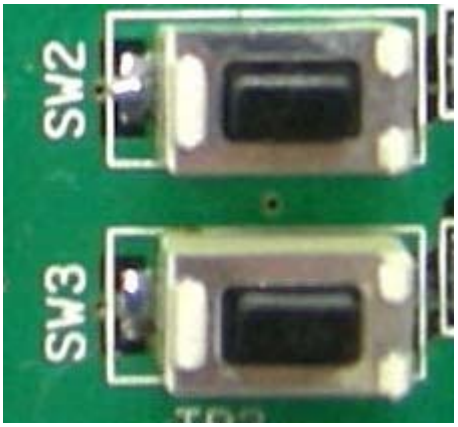
SW 2 and SW 3 are push switches. There are connecting to pull-up resister. It becomes "Low", while they are being pushed. and It becomes "High" if the switch separate,

SW2,SW3 terminal list (ALPS SKQMBBE010)

	Signal name	Terminal CPU name at connection destination	Notes
SW2	P50	P50/TIQ01/TOQ01/RTP00/KR0	
SW3	P51	P51/TIQ02/TOQ02/RTP01/KR1	

SW2

SW3



2.3 SW4

SW4 is the reset switch. CPU can be reset by pushing.

SW4

2.4 LED5

`Power LED'. LED1 is activated when the power supply is turned on.

2.5 LED1, LED2, LED3, LED4

LED1,2,3 and 4 are available for applications. To make an LED on, please set the output port LOW.

LED1,LED2,LED3 and LED4 terminal list (STANLEY ELECTRIC　PG1111C)

	Signal name	Terminal CPU name at connection destination	Notes
LED1	PDH0	PDH0	
LED2	PDH1	PDH1	
LED3	PDH3	PDH3	
LED4	PDH2	PDH2	

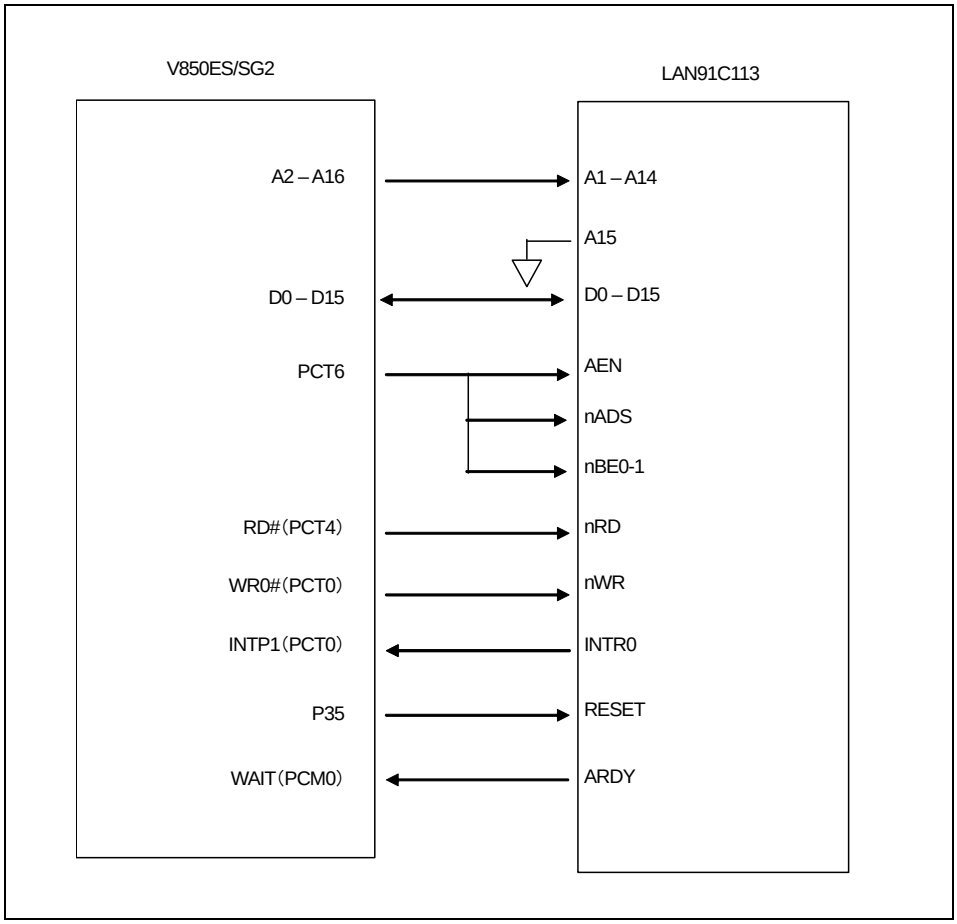
LED1
LED2
LED3
LED4

3 LAN Controller

CPU board has a LAN controller, LAN91C113 made by SMSC.

3.1 Connection

Connection of CPU to LAN controller is below.



3.2 Reset of LAN Controller

P35 is used to make a reset of LAN controller. When P35 will be Hi-z after CPU reset, LAN controller will be reset state, Before release the reset, Please change the CPU port "Chip Select Signal (AEN,nADS)" and "Read/Write Signal" to be inactive level. And then drive the P35 to Low. and release the reset.

The MAC address is initialized to the contents of EEPROM, after release the reset.

3.3 Access to the LAN Controller

It is need to set external bus to separate mode for accessing to the LAN Controller.

LAN controller address is connected to CPU address on the 1bit shift. So LAN controller resister mapped on skip over 2 Words (4Byte). Also it cannot Byte access to LAN controller, because nBE and nBE1 signal make low level at the same timing.

The Chip Select (AEN, nADS) of LAN controller uses the port, Please make the low level when access to LAN controller. and If access ends, make high level.

4 Temperature Sensor

CPU board has a temperature sensor for measure ambient of PWB board, that is connecting to analog input pin （P79/ANI9） of CPU

- Temperature sensor　S-8120C (Made by SII)
- Power Supply of sensor ：+3.3V
- Linear output voltage(Please refer to data sheet about details.)

  -8.20mV/℃ (-20℃～80℃)

5 Power Supply

There are two choices to supply power to the board, USB or a 006P battery via CN2. Please refer to 2.1.4 JP1 for the jumper setting.

Please replace the battery with a new one, if the voltage level goes down to 4.75V.

Below the voltage level of 4.75V, functions of the board are not guaranteed.

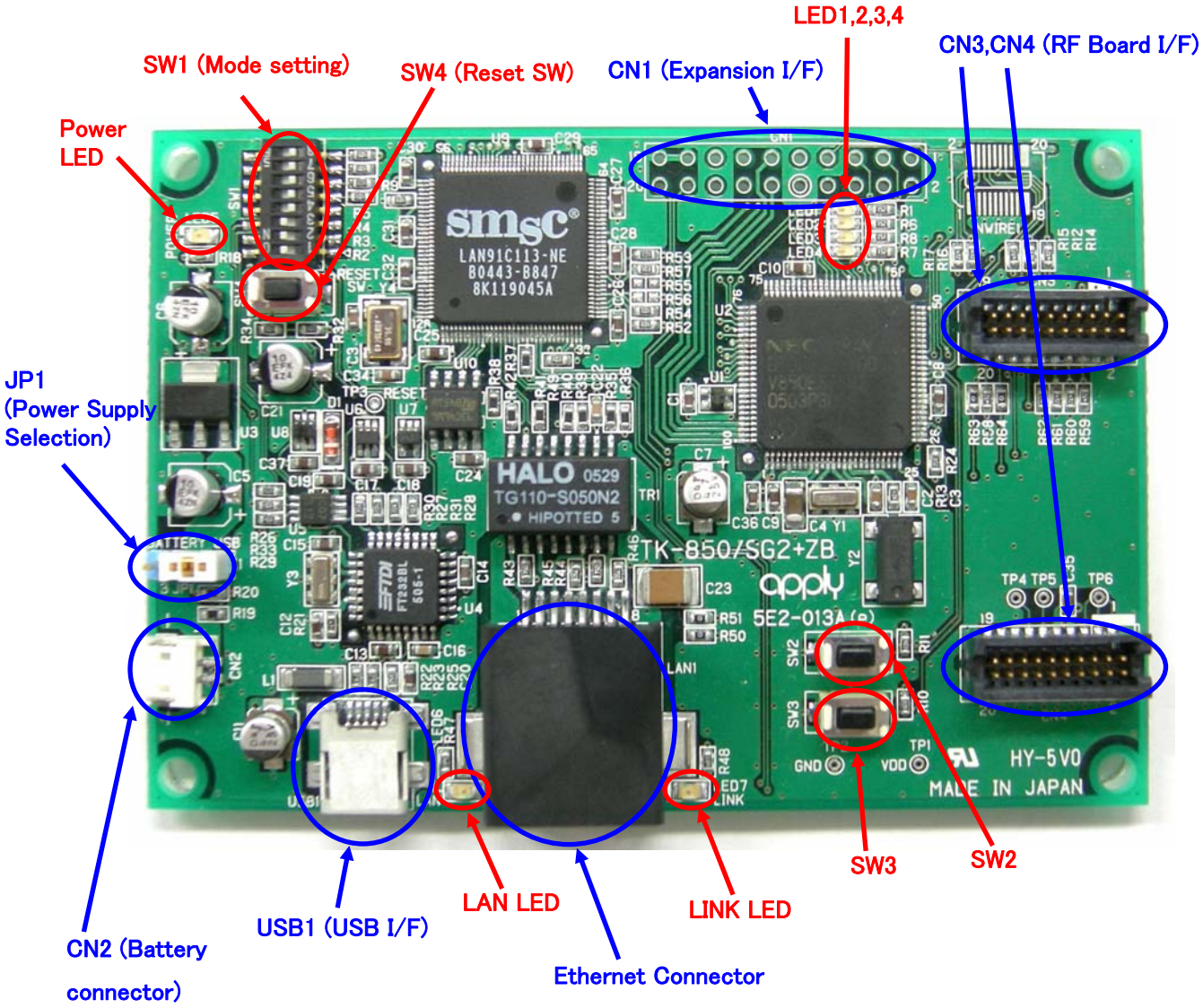
The battery voltage can be checked at the port as shown below.

9.0V Battery check

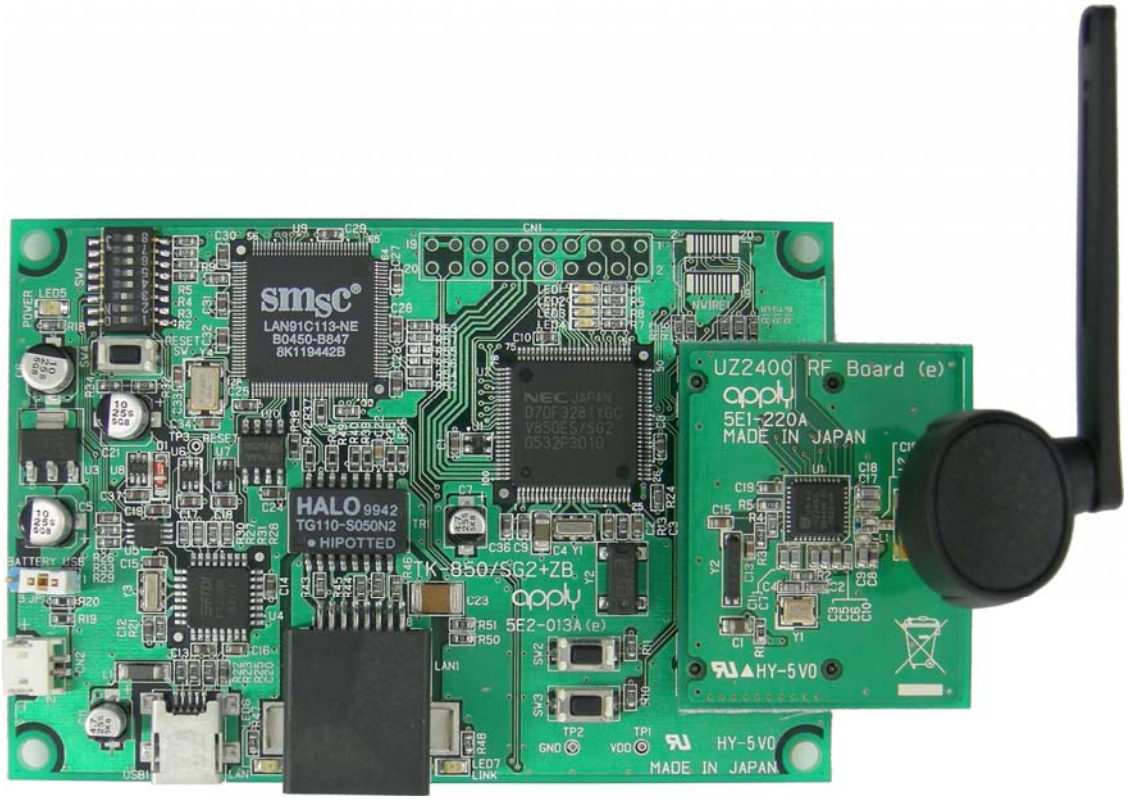
Signal name	Terminal CPU name at connection destination	Notes
BT_MONI	P78/ANI8	About 0.265 times of input power supply For instance If the battery level 6.0V: The level of the BT_MONI=0.265×6.0 =1.59(V) If the battery level is 4.75V: The level of the BT_MONI=0.265×4.75 =1.25(V)

6 TK-850/SG2+UZ Data

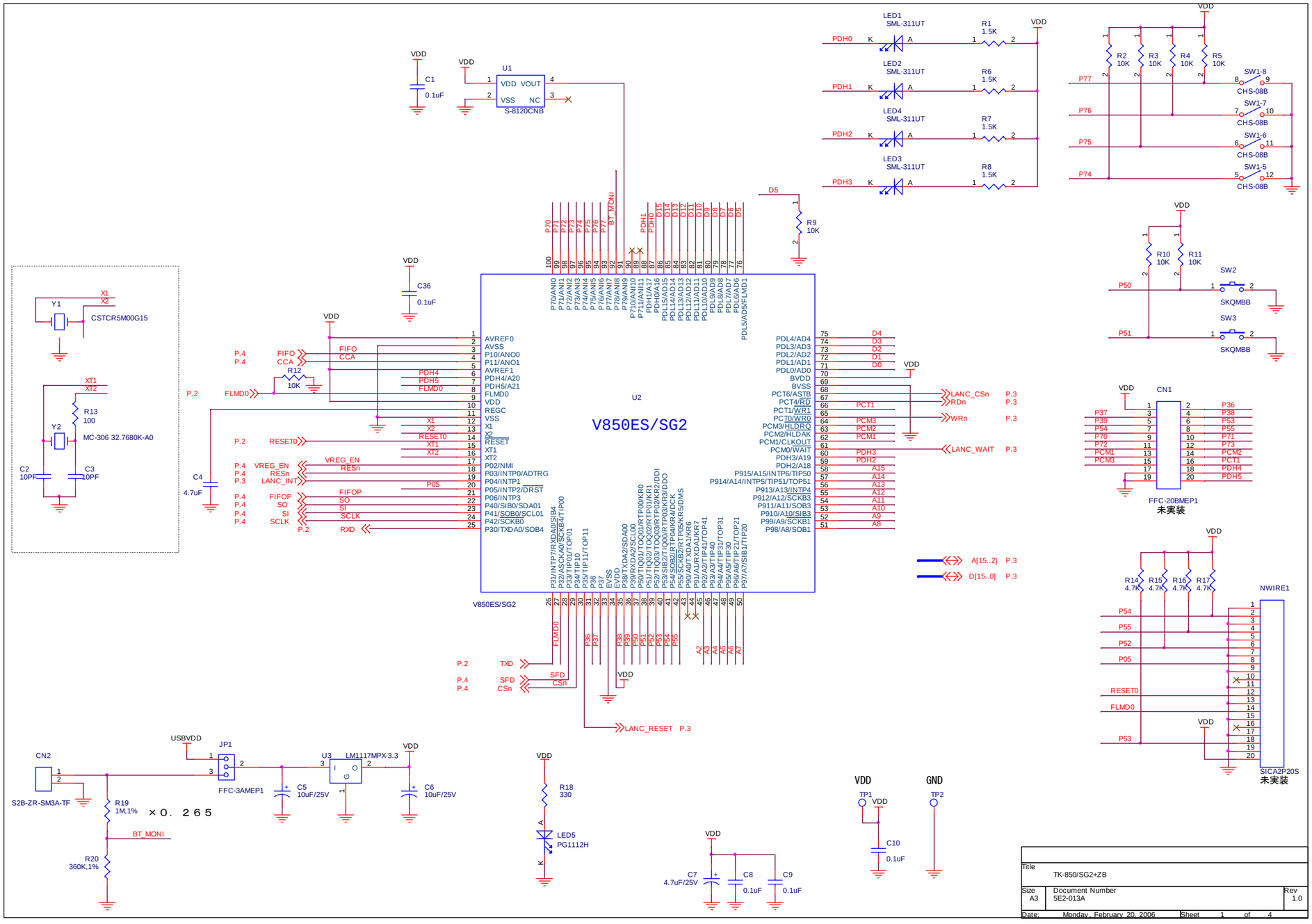
6.1 Parts layout

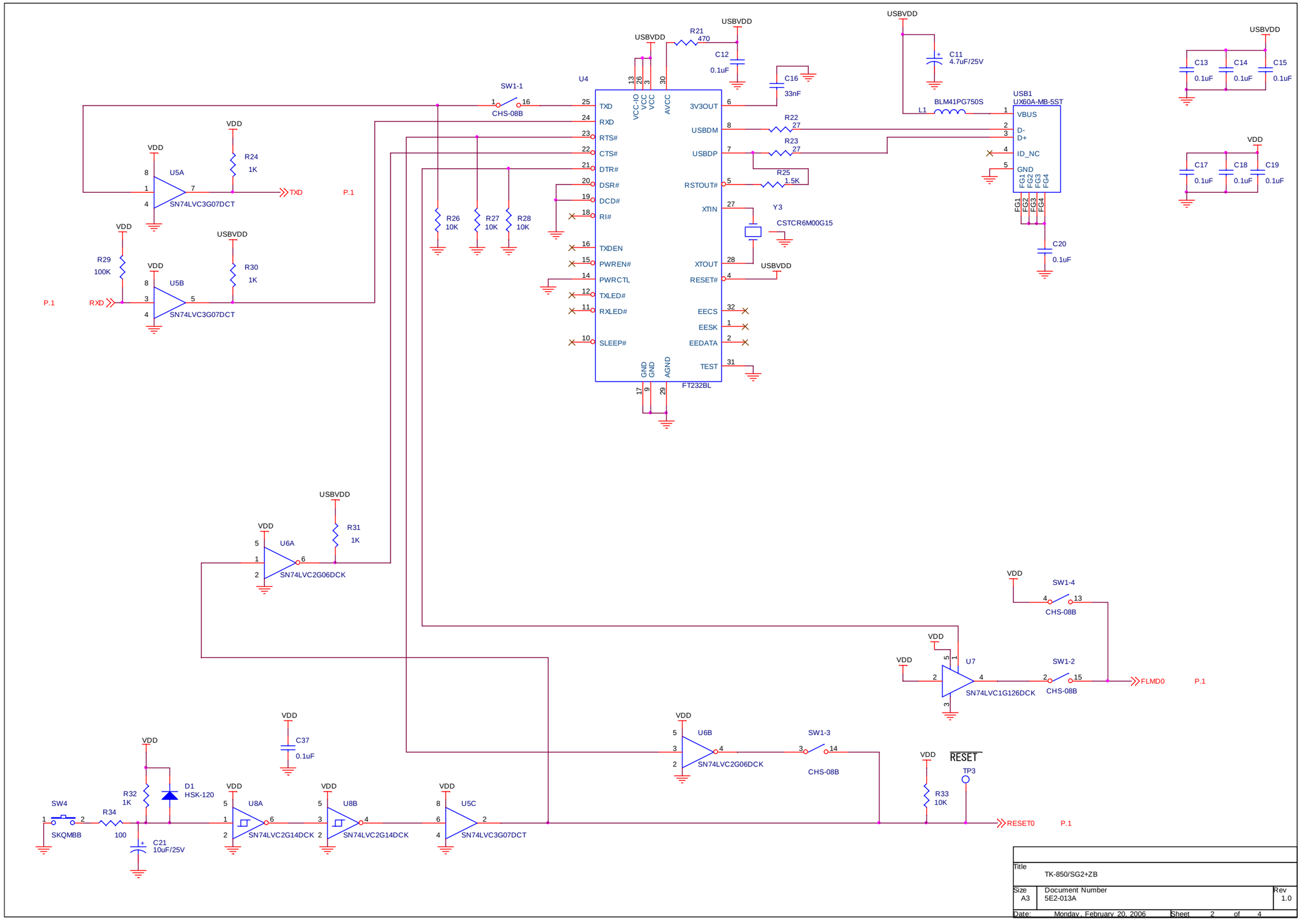


6.2 RF Board connection figure



6.3 Circuit Diagram of the CPU Board





Title	TK-850/SG2+ZB	
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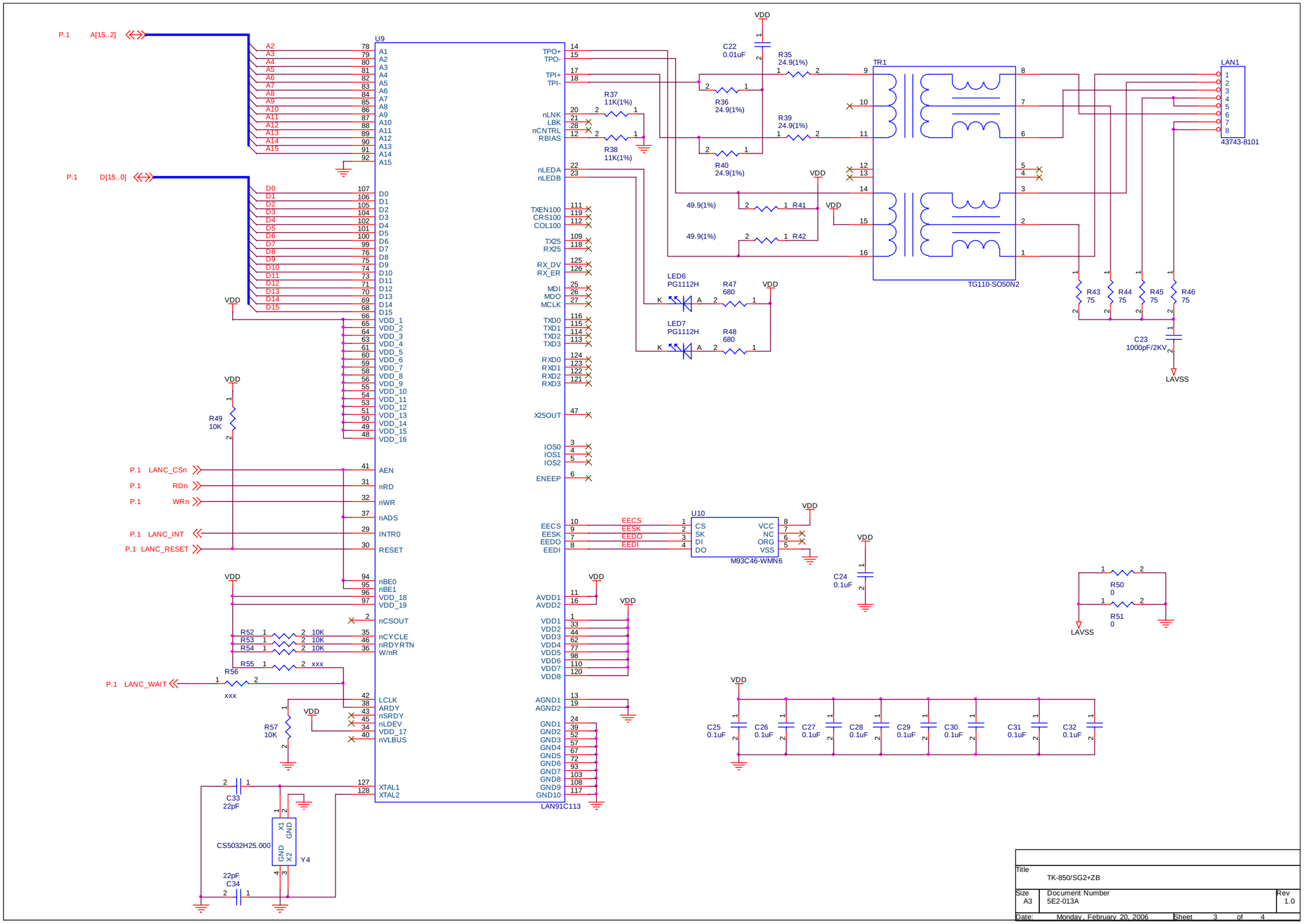
U9
LAN91C113
P.1 A[15..2]
P.1 D[15..0]
P.1 LANC_CSn
P.1 RDn
P.1 WRn
P.1 LANC_INT
P.1 LANC_RESET
P.1 LANC_WAIT
AEN
nRD
nWR
nADS
INTR0
RESET
nBE0
nBE1
nCSOUT
nCYCLE
nRDYRTN
W/nR
LCLK
ARDY
nSRDY
nLDEV
nVLBUS
XTAL1
XTAL2
TPO+
TPO-
TPI+
TPI-
nLNK
LBK
nCNTRL
RBIAS
nLEDA
nLEDB
TXEN100
CRS100
COL100
TX25
RX25
RX_DV
RX_ER
MDI
MDO
MCLK
TXD0
TXD1
TXD2
TXD3
RXD0
RXD1
RXD2
RXD3
X25OUT
IOS0
IOS1
IOS2
ENEEP
VDD
R37 11K(1%)
R38 11K(1%)
R35 24.9(1%)
R36 24.9(1%)
R39 24.9(1%)
R40 24.9(1%)
C22 0.01uF
TR1
TG110-SO50N2
LAN1
43747-8101
49.9(1%)
R41
R42
LED6 PG1112H
LED7 PG1112H
R47 680
R48 680
R43 75
R44 75
R45 75
R46 75
C23 1000pF/2KV
LAVSS
R49 10K
R52 10K
R53 10K
R54 10K
R55 xxx
R56 xxx
R57 10K
C33 22pF
C34 22pF
CS5032H25.000
Y4
U10
M93C46-WMN6
EECS
EESK
EEDO
EEDI
C24 0.1uF
R50 0
R51 0
AVDD1
AVDD2
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
AGND1
AGND2
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
C25 0.1uF
C26 0.1uF
C27 0.1uF
C28 0.1uF
C29 0.1uF
C30 0.1uF
C31 0.1uF
C32 0.1uF
Title
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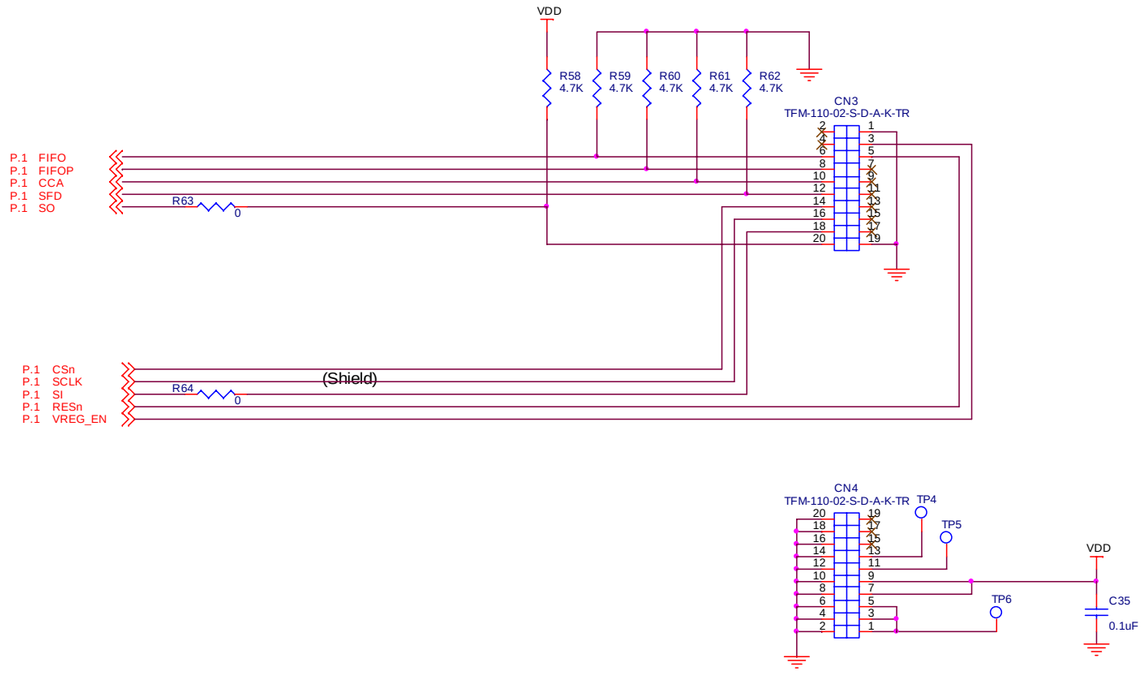

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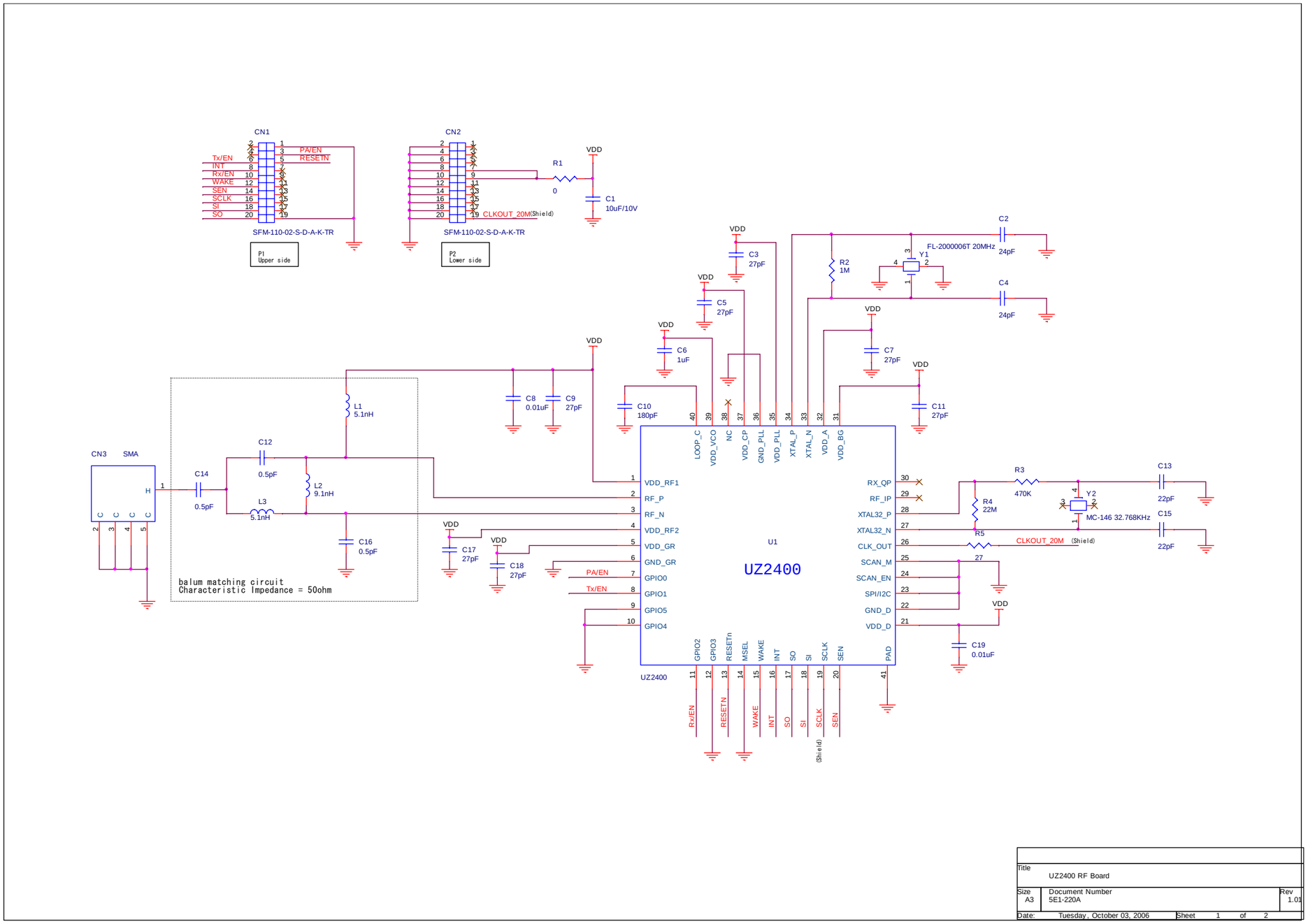
6.4 Circuit Diagram of the UZ2400 RF board



6.5 Dimension of the CPU board